

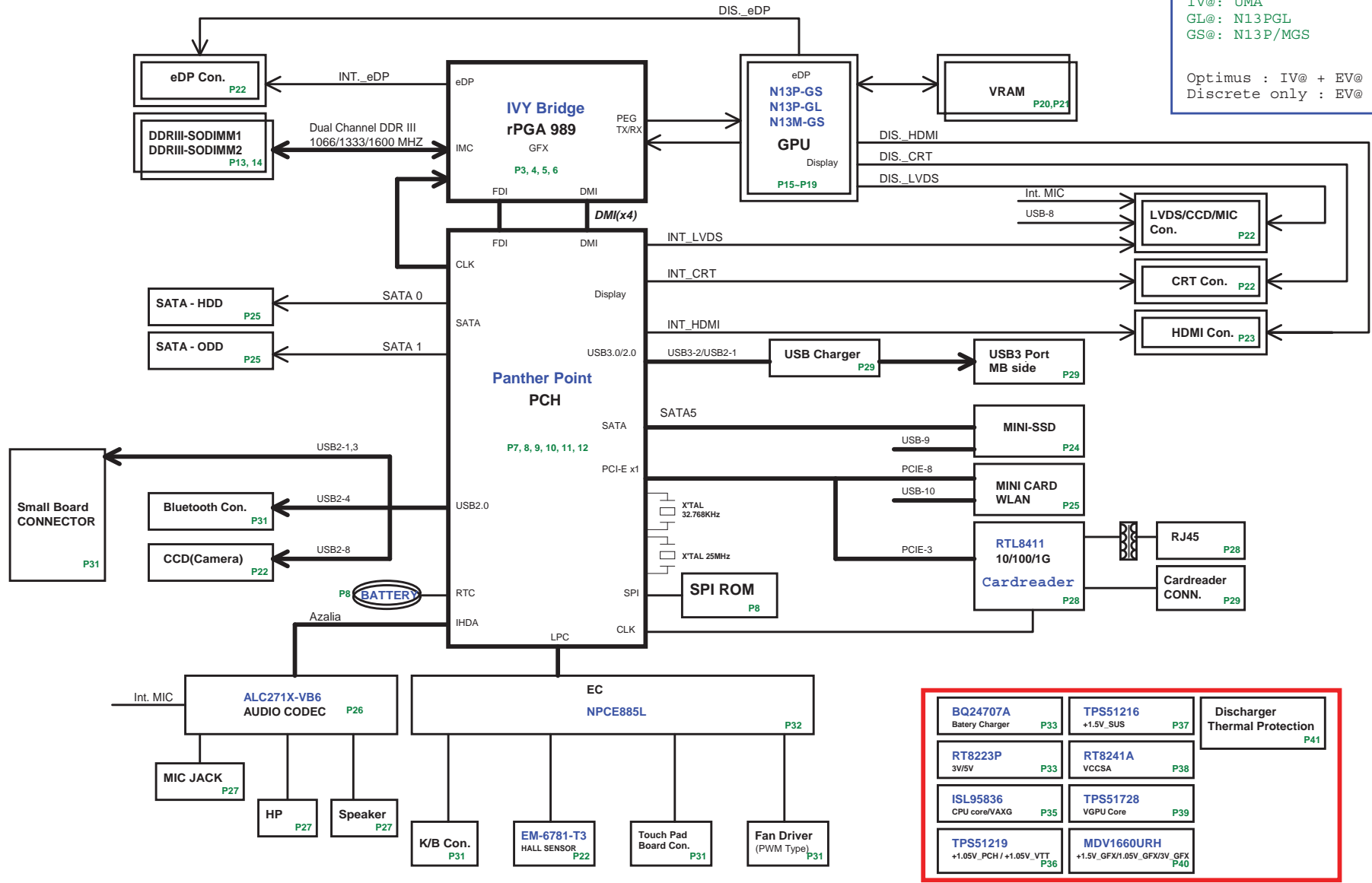
# ZQTA/ZQSA CRV SYSTEM BLOCK DIAGRAM

**BOM**

**Vinafix**

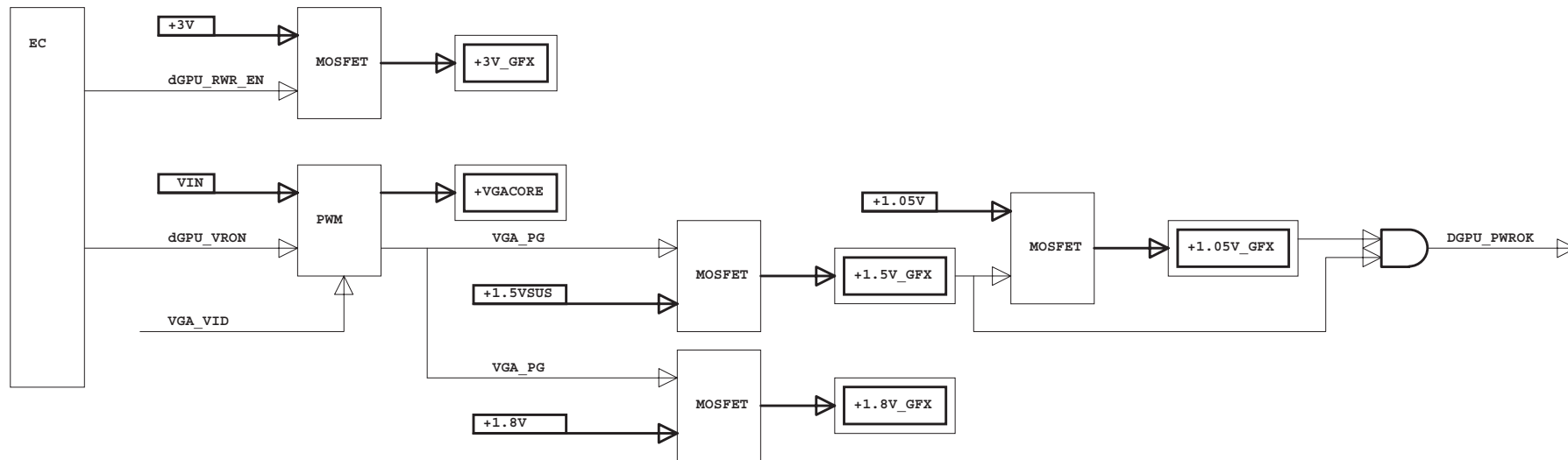
V@ : 1.5V\_PCH  
 EV@ : 1.5V\_PCH  
 OP@ : 1.5V\_PCH  
 DO@ : Discrete only  
 SP@ : 1.5V\_PCH  
 SNP@ : N13PGS/GL  
 IV@ : UMA  
 GL@ : N13PGL  
 GS@ : N13P/MGS

Optimus : IV@ + EV@ + OP@  
 Discrete only : EV@ + DO@



[www.vinafix.vn](http://www.vinafix.vn)

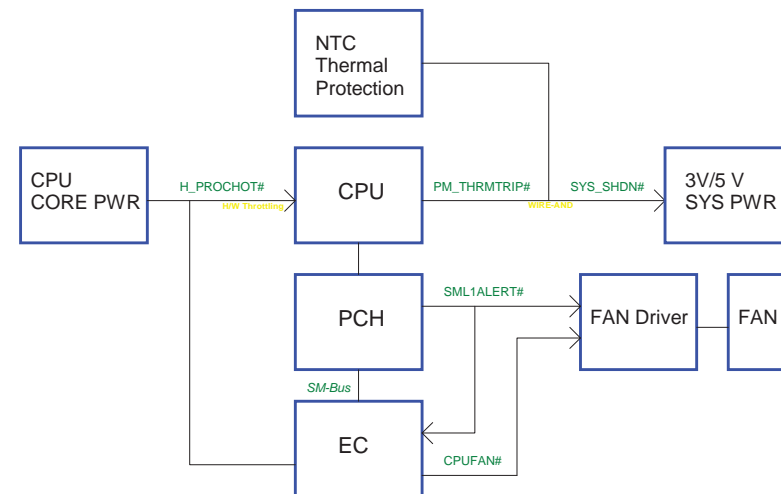
### VGA power up sequence



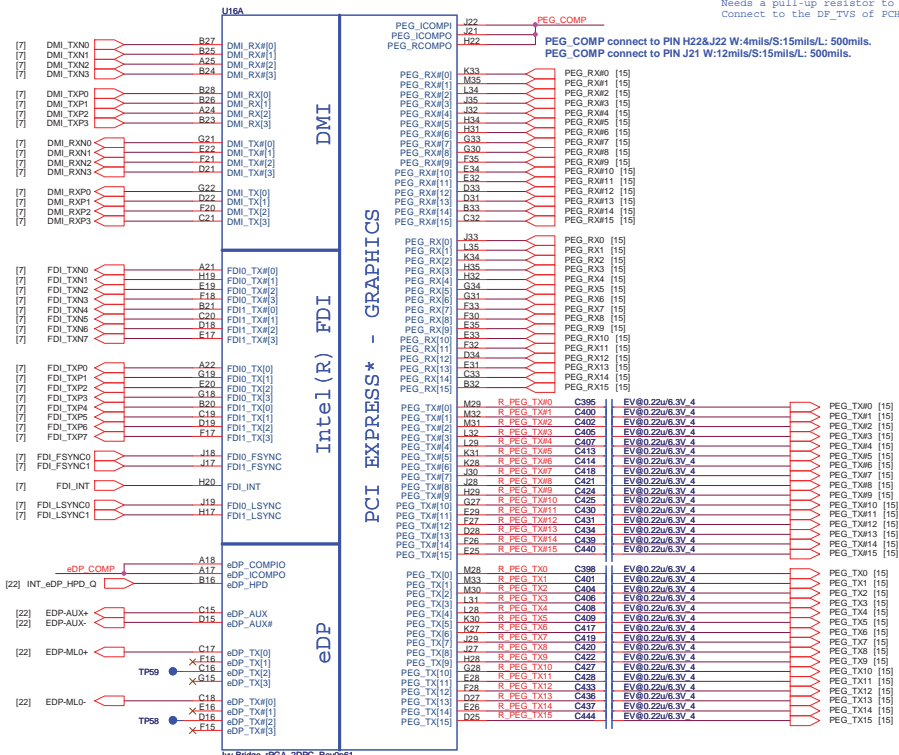
## Power States

POWER PLANE	VOLTAGE	DESCRIPTION	CONTROL SIGNAL	ACTIVE IN
VIN	+10V~+19V	MAIN POWER	ALWAYS	ALWAYS
+3V_RTC	+3V~+3.3V	RTC POWER	ALWAYS	ALWAYS
+3VPCU	+3.3V	EC POWER	ALWAYS	ALWAYS
+5VPCU	+5V	CHARGE POWER	ALWAYS	ALWAYS
+15V	+15V	CHARGE PUMP POWER	ALWAYS	ALWAYS
+3V_S5	+3.3V	LAN/BT/CIR POWER	S5_ON	S0-S5
+5V_S5	+5V	USB POWER	S5_ON	S0-S5
+5V	+5V	HDD/ODD/Codec/TP/CRT/HDMI POWER	MAINON	S0
+3V	+3.3V	PCH/GPU/Peripheral component POWER	MAINON	S0
+1.5VSUS	+1.5V	CPU/SODIMM CORE POWER	SUSON	S0-S3
+0.75V_DDR_VTT	+0.75V	SODIMM Termination POWER	MAINON	S0
+VGFX_AXG	variation	Internal GPU POWER	VRON	S0
+1.8V	+1.8V	CPU/PCH/Braidwood POWER	MAINON	S0
+1.5V	+1.5V	MINI CARD/NEW CARD POWER	MAINON	S0
+1.05V	+1.05V	PCH CORE POWER/IVY/SNB bridge VCCIO	MAINON	S0
+VCCSA	+0.9V	CPU POWER	HWP_G_VTT	S0
+VCC_CORE	variation	CPU CORE POWER	VRON	S0
LCDVCC	+3.3V	LCD POWER	LVDS_VDDEN	S0
			MAINON	S0

### Thermal Follow Chart



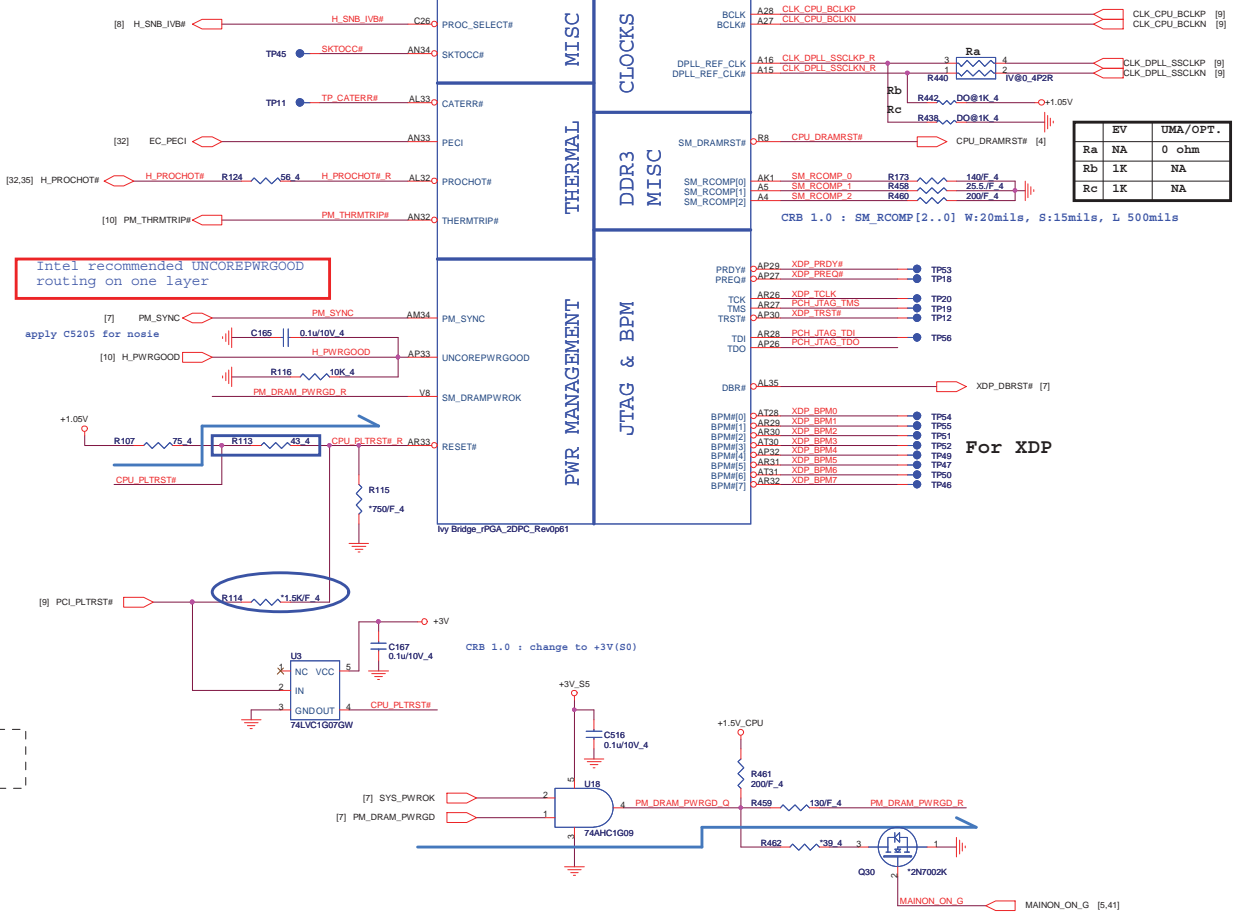
# IVY Bridge Processor (DMI, PEG, FDI)



For Sandy Bridge processor only implementation:  
PROC\_SELECT can be left NC.

For IVY/Sandy processor compatibility:  
Needs a pull-up resistor to PCH VocDPTERM rail (1.8V) through a 2.2 K $\Omega$ ±5% pull-up resistor.  
Connect to the DP\_VIS of PCH through a 1K $\Omega$ ±5% series resistor.

# IVY Bridge Processor (CLK, MISC, JTAG)



wo eDP and dGPU  
Connect DPLL\_REF\_SSCLK on Processor to GND through 1K  $\pm$  5% resistor.  
Connect DPLL\_REF\_SSCLK# on Processor to VCCP through 1K  $\pm$  5% resistor.

Intel recommended UNCOREPWRGOOD routing on one layer

apply C5205 for noise

R114 1.5K $\Omega$  4

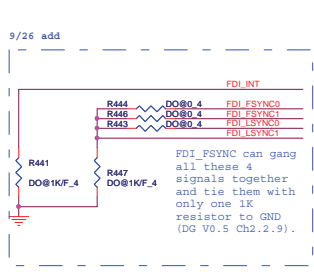
CRB 1.0 : change to +3V(S0)

For XDP

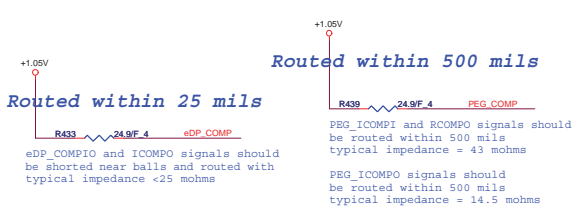
**HPD disable**  
This signal can be left as no connect if entire eDP interface is disabled.

**CRB 1.0 :**  
The recommended AC cap value is changed to 220nF for compatibility with PCIe Gen3 on future platforms.  
For Gen2 only designs, it is acceptable to continue to use the 100nF capacitor.

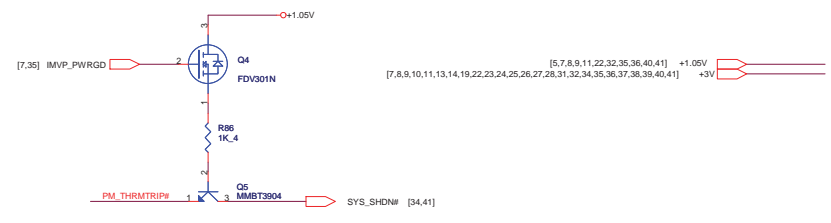
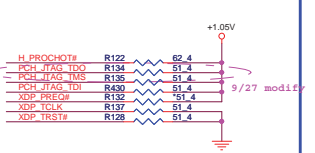
## FDI Disabling (Discrete Only)



## DP & PEG Compensation



## Processor pull-up(CPU)

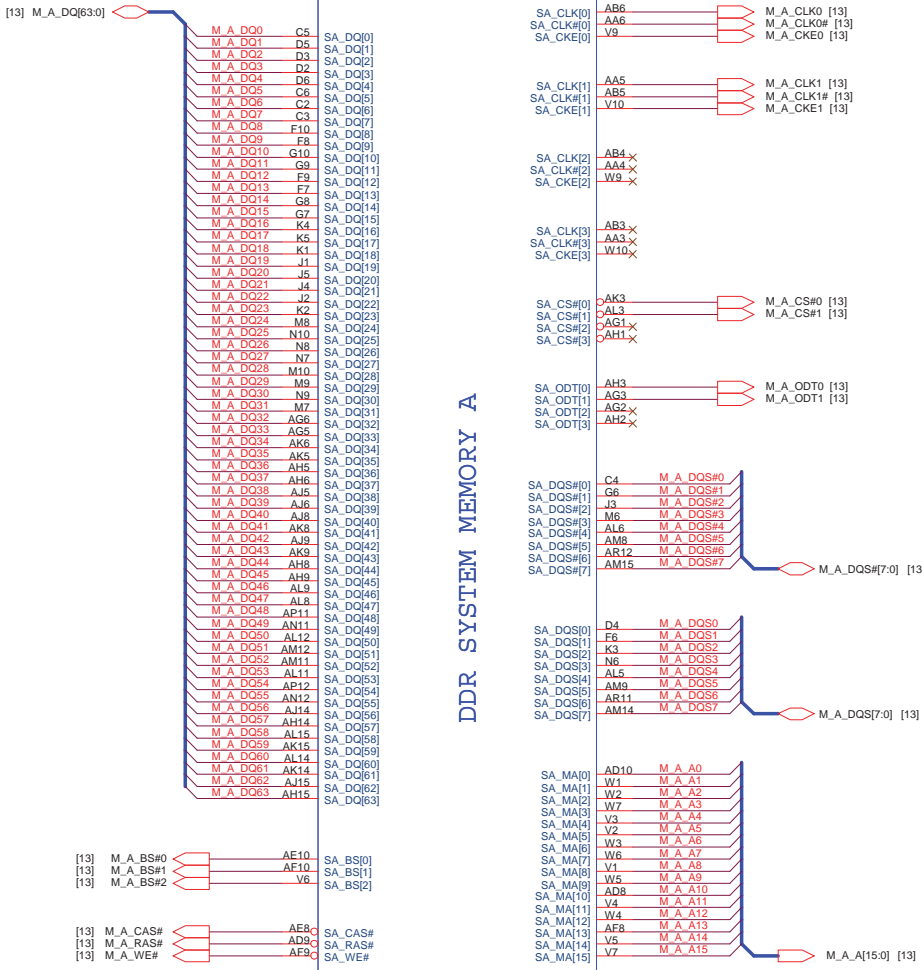


# IVY Bridge Processor (DDR3)

U16C

Ivy Bridge\_rPGA\_2DPC\_Rev0p61

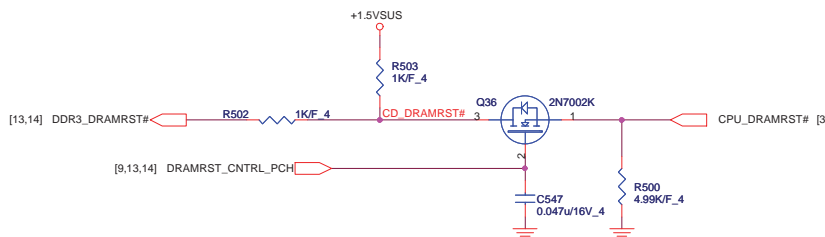
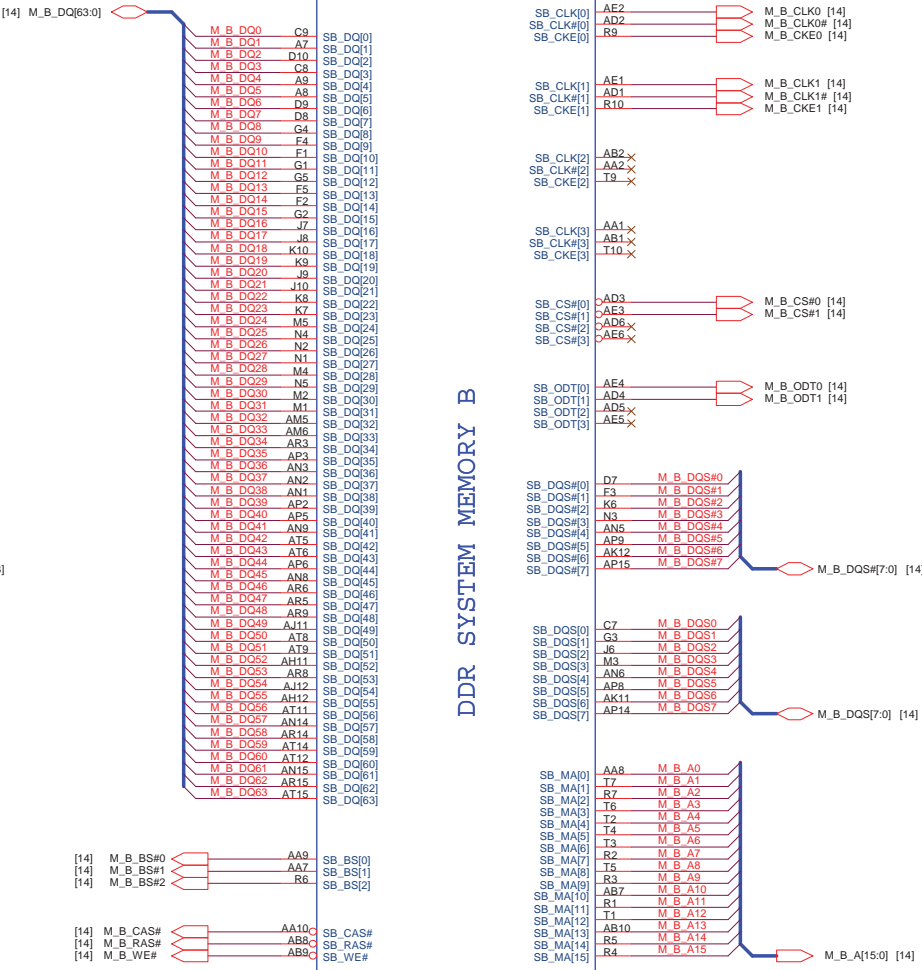
DDR SYSTEM MEMORY A



U16D

Ivy Bridge\_rPGA\_2DPC\_Rev0p61

DDR SYSTEM MEMORY B

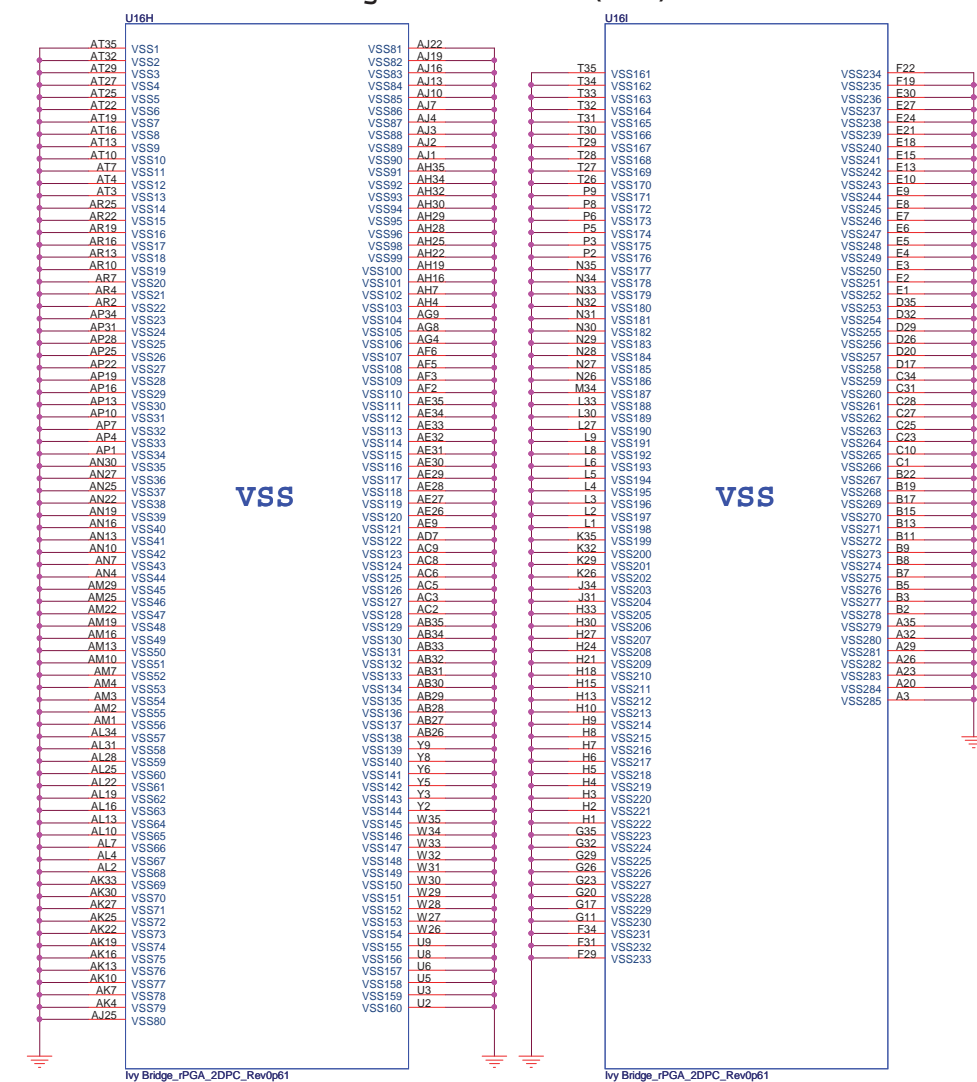


**Quanta Computer Inc.**  
PROJECT : ZQTA/ZQSA

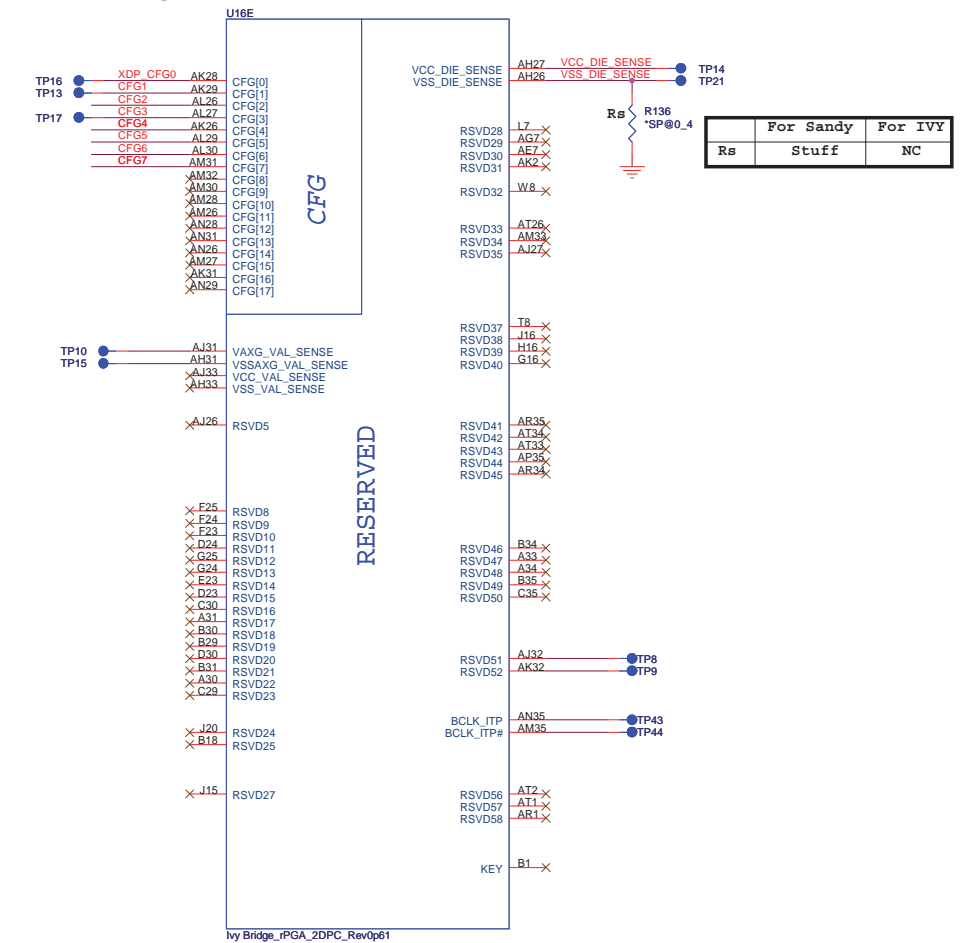
Size	Document Number	Rev
	IVY Bridge 2/4	1A
Date:	Friday, November 11, 2011	Sheet 4 of 44



# IVY Bridge Processor (GND)



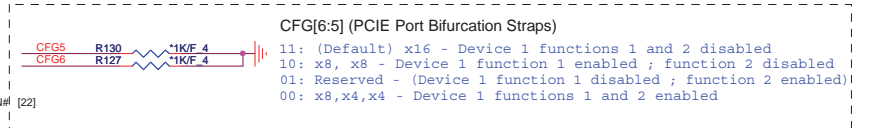
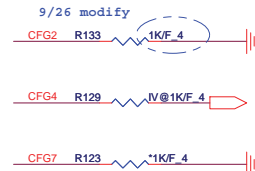
# IVY Bridge Processor (RESERVED, CFG)



## Processor Strapping

The CFG signals have a default value of '1' if not terminated on the board.

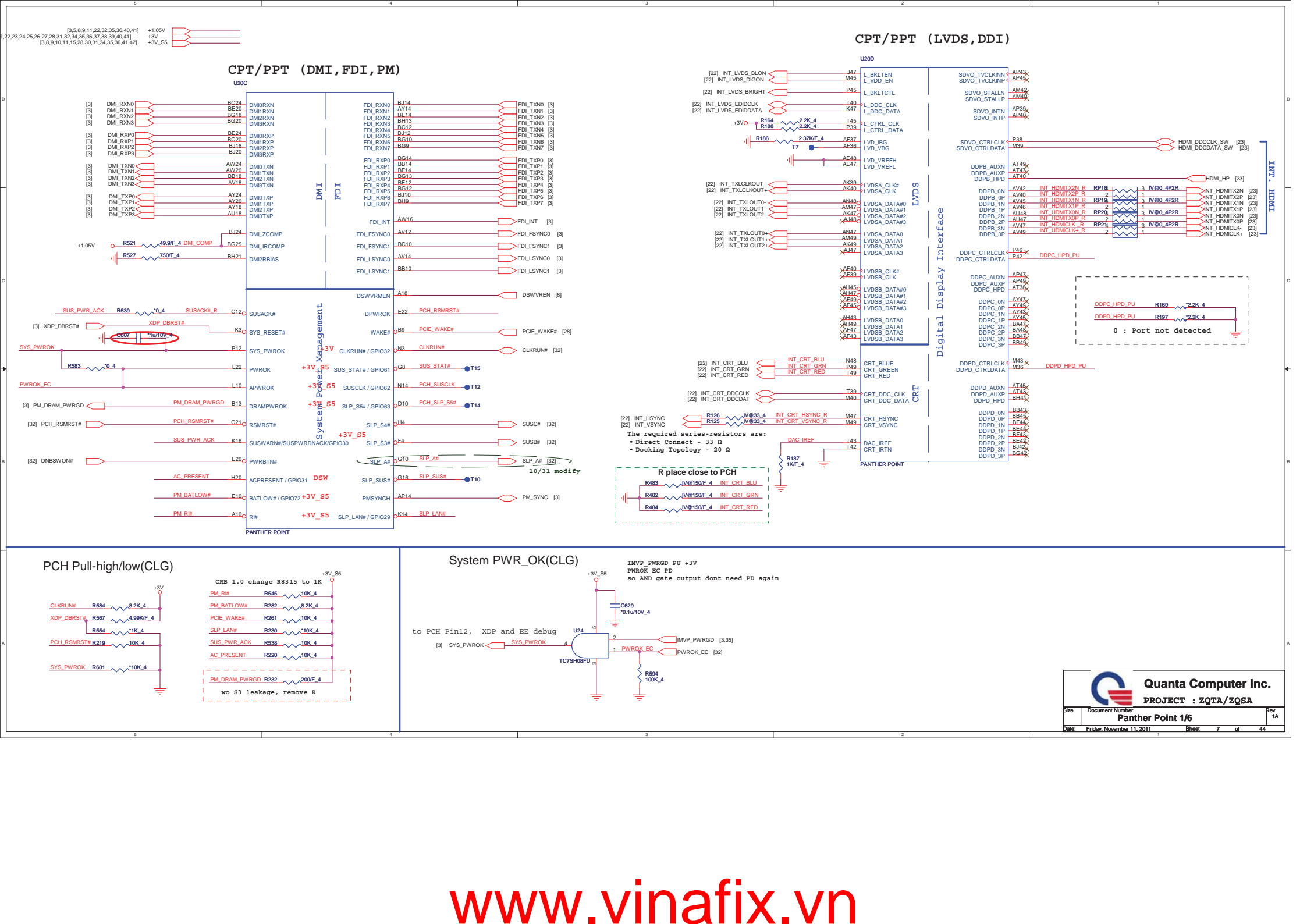
	1	0
CFG2 (PEG Static Lane Reversal)	Normal Operation	Lane Reversed
CFG4 (DP Presence Strap)	Disable; No physical DP attached to eDP	Enable; An ext DP device is connected to eDP
CFG7 (PEG Defer Training)	PEG train immediately following xxRESETB de assertion	PEG wait for BIOS training



**Quanta Computer Inc.**  
PROJECT : ZQTA/ZQSA

Size	Document Number	Rev
	<b>IVY Bridge 4/4</b>	1A
Date:	Friday, November 11, 2011	Sheet 6 of 44

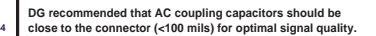




20mils



PCH2 (CLG)



### PCH Strap Table

Used as GPIO only. at chklist 1.2

**Default weak pull-up on GNT0/1#**  
**[Need external pull-down for LPC BIOS]**

ME WR default EC setting folating

for future CPU, Sandy Bridge NC  
DF\_TVS needs to be pulled up to VccDFTERM power rail  
through 2.2 kOhm  $\pm 5\%$  - R8361 change to 0 or not??

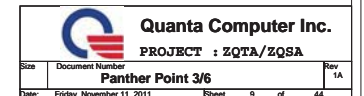
Needs to be pulled High for Huron River platform.  
chklist 1.2

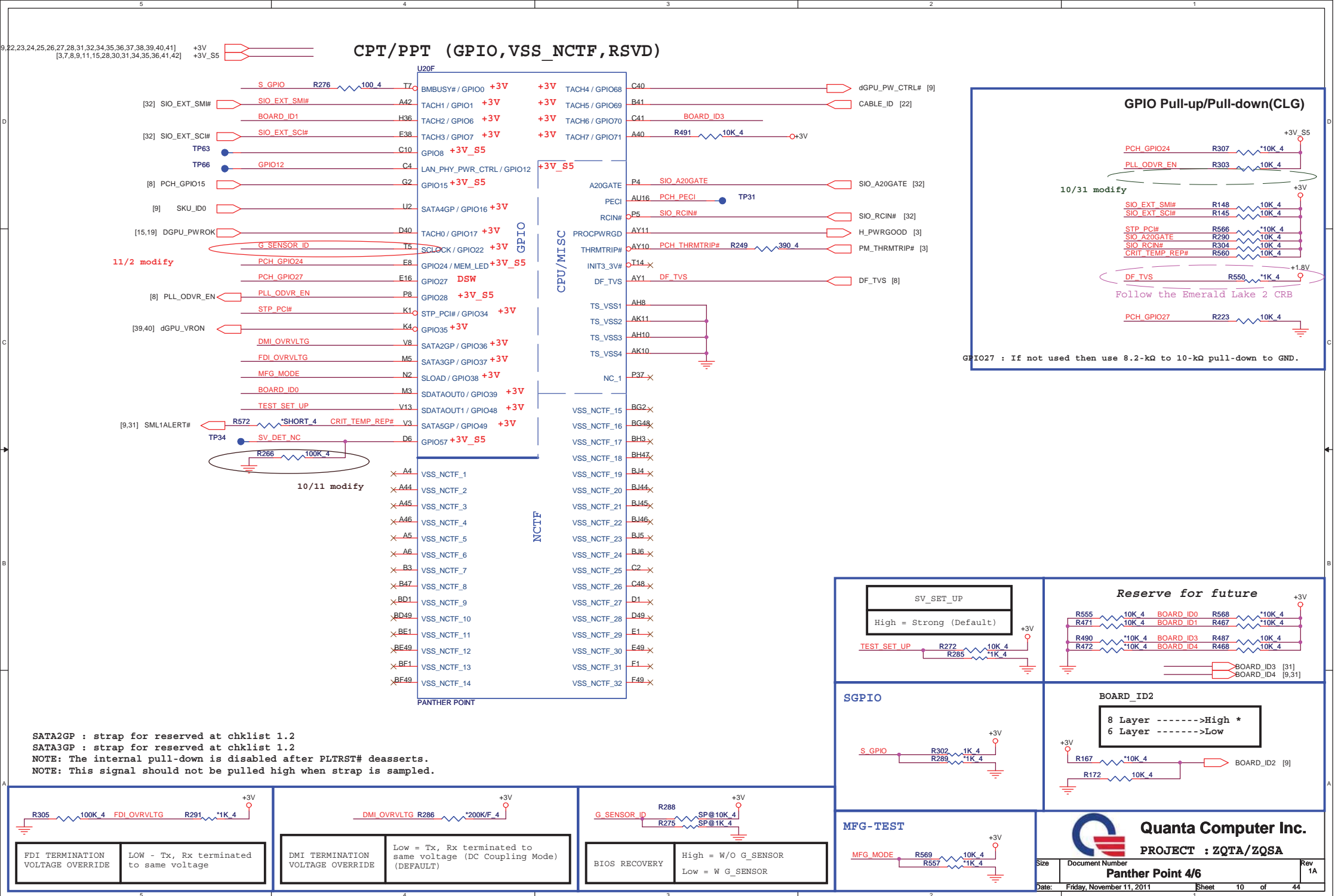


## U20

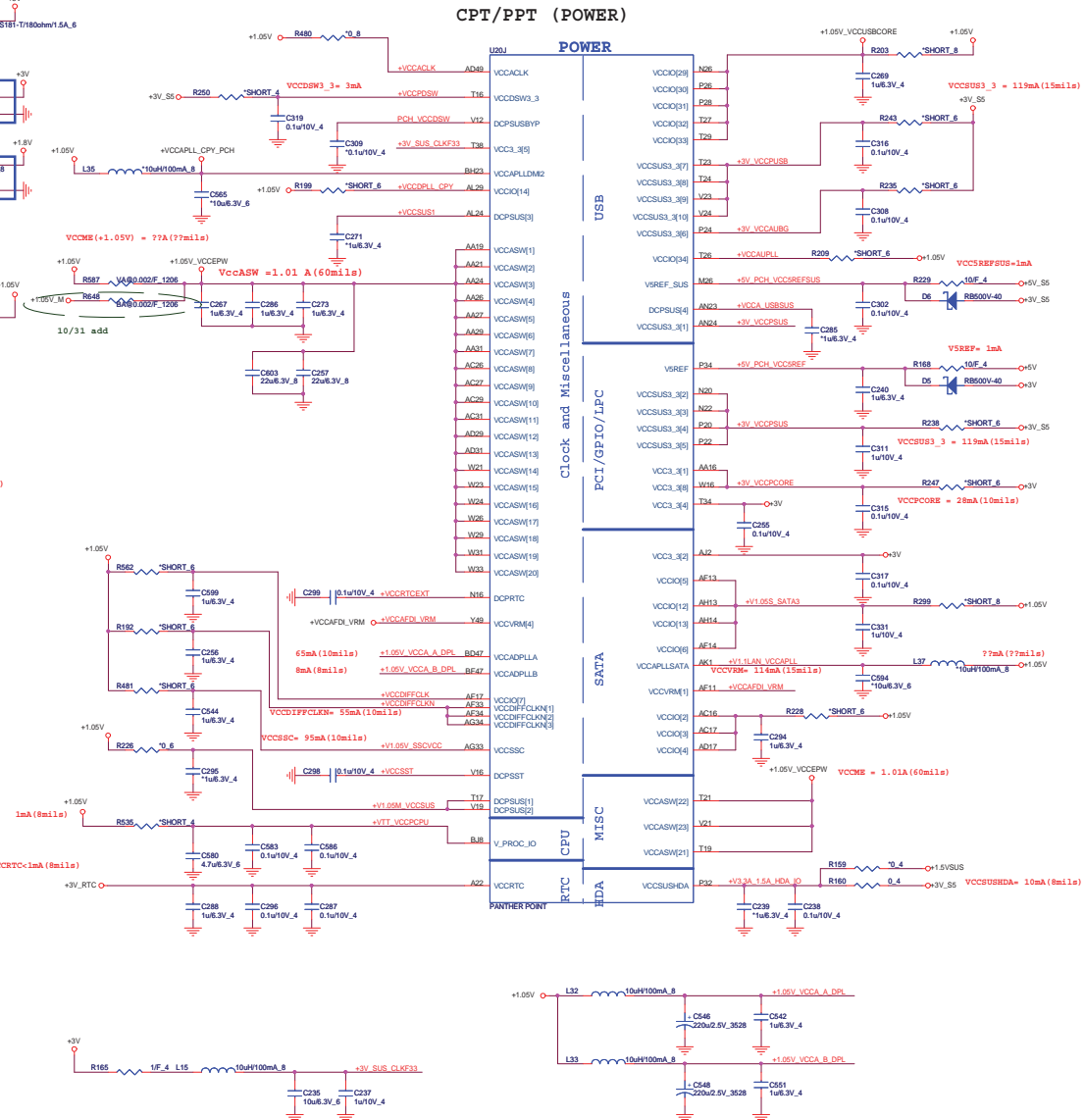
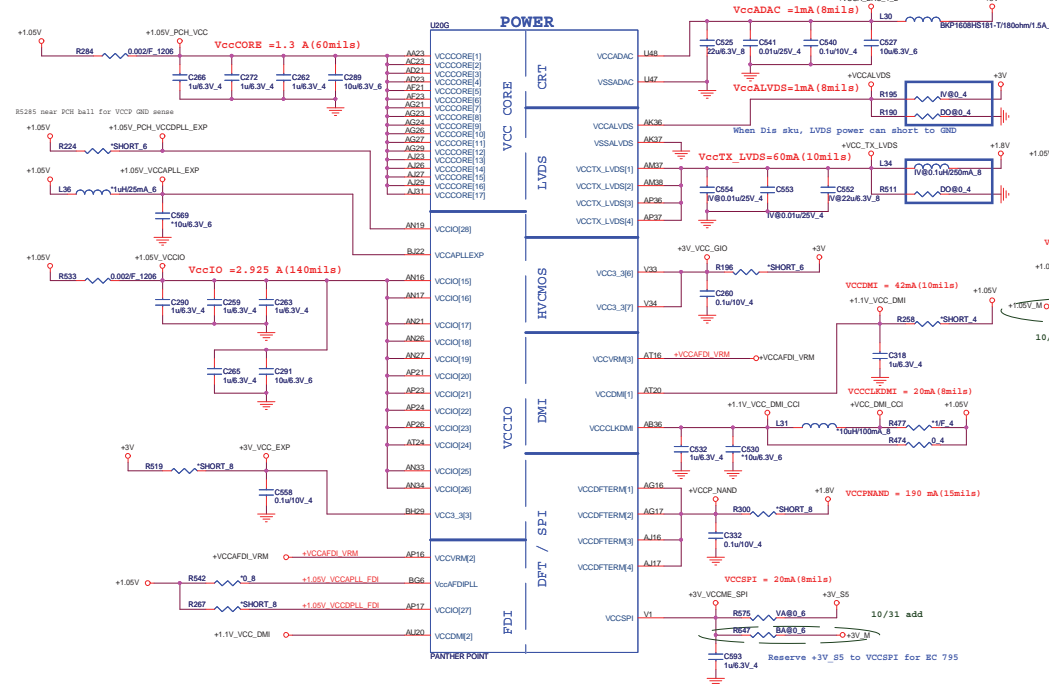


## SMBus(PCH)

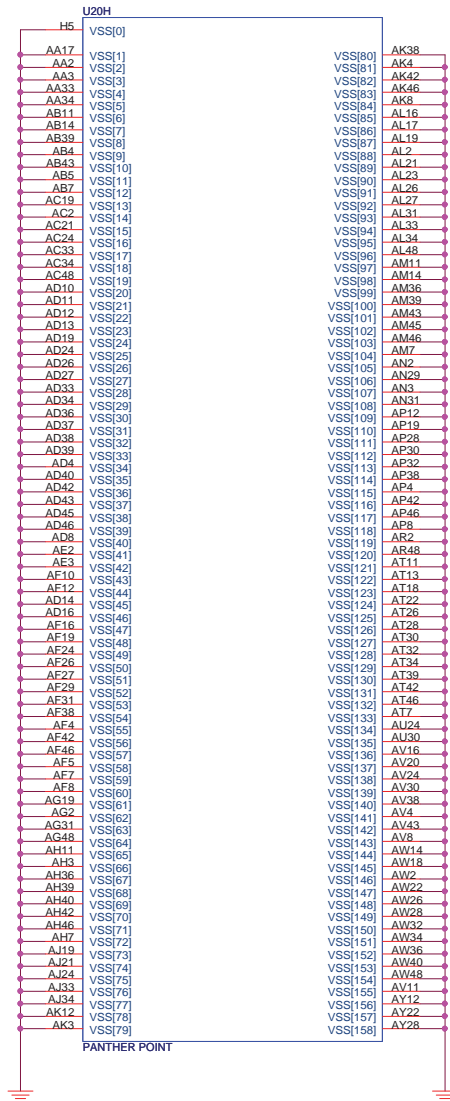




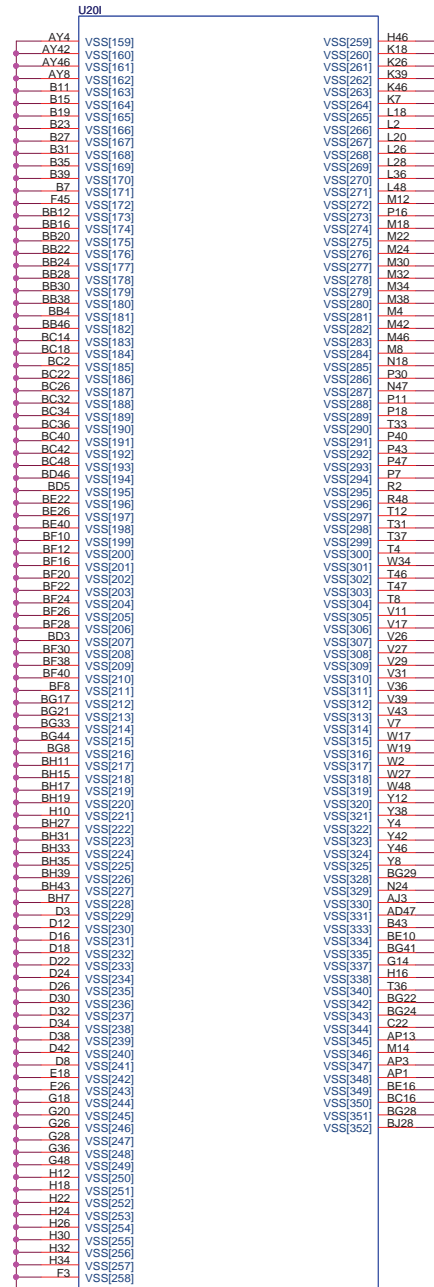
## CPT/PPT (POWER)



## IBEX PEAK-M (GND)



PANTHER POINT



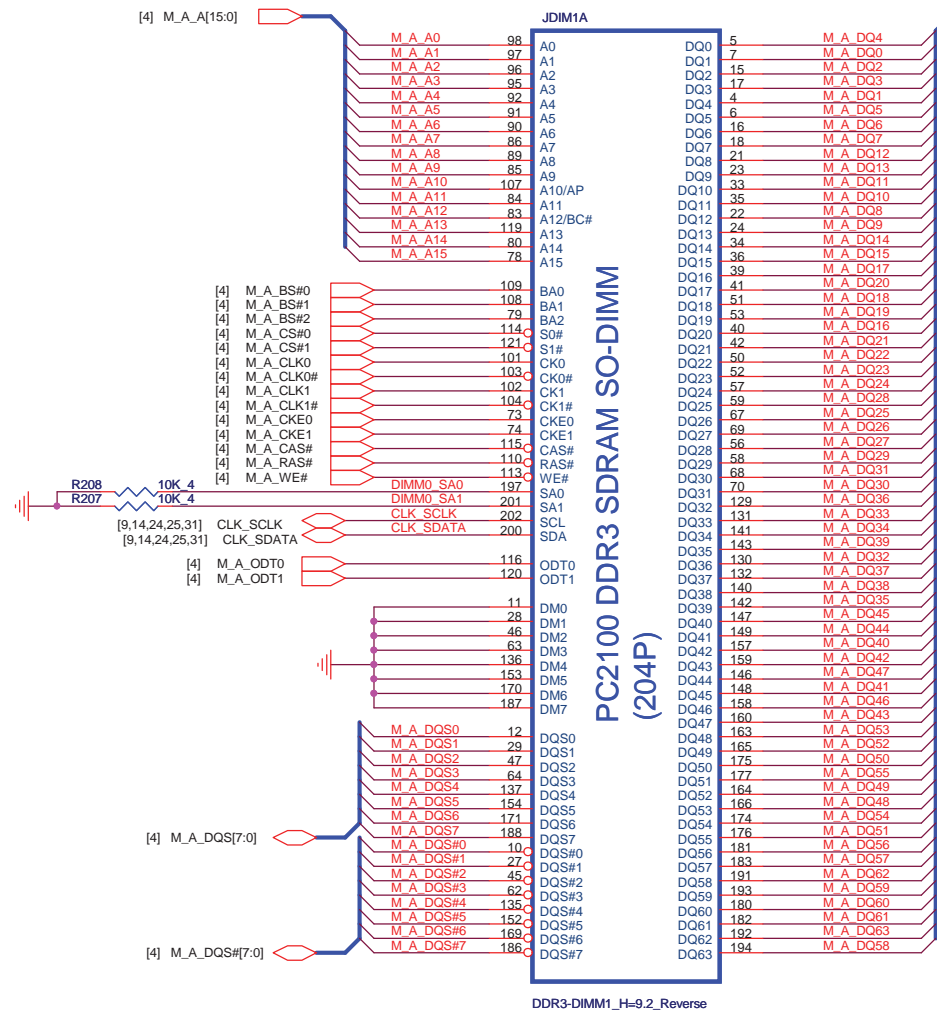
PANTHER POINT



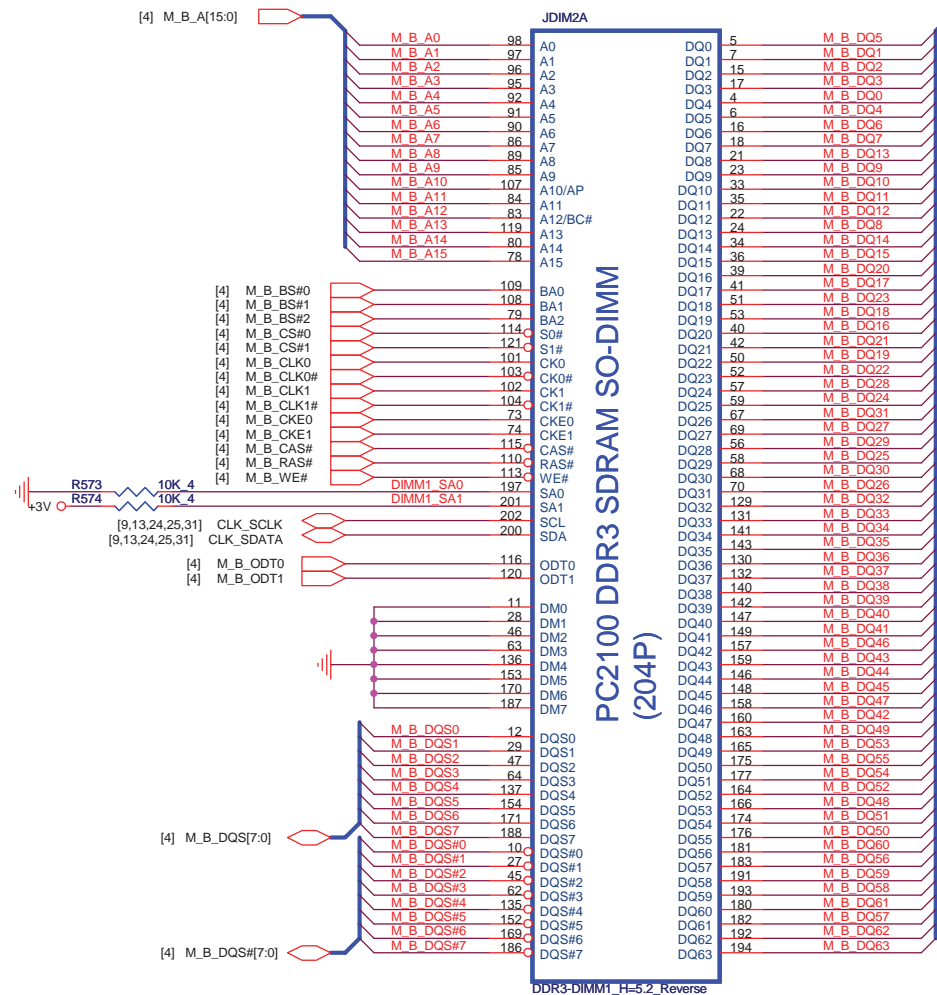
Quanta Computer Inc.

PROJECT : ZQTA/ZQSA

Doc Number	Panther Point 6/6	Rev	1A
Date	Friday, November 11, 2011	Sheet	12 of 44





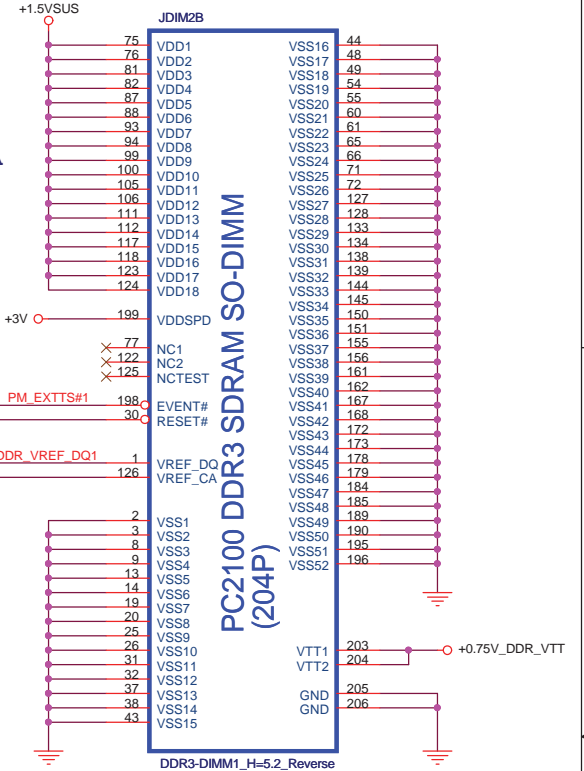


M3 solution

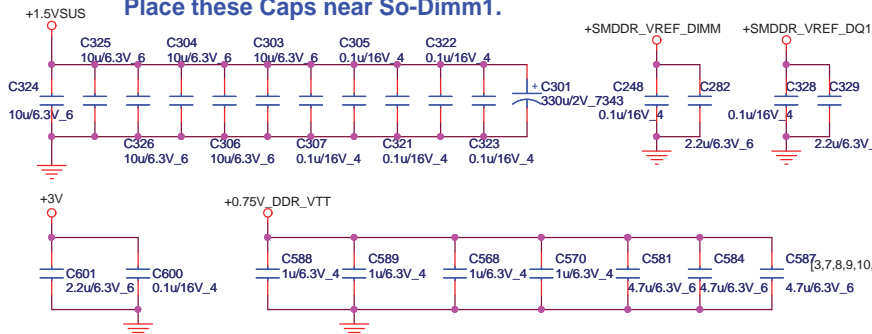
[5] SMDDR\_VREF\_DQ1\_M3



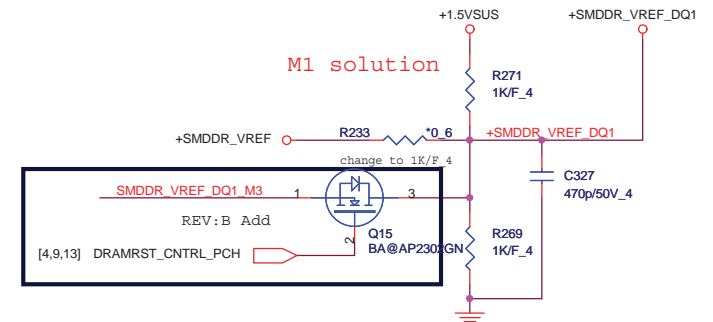
2.48A



Place these Caps near So-Dimm1.

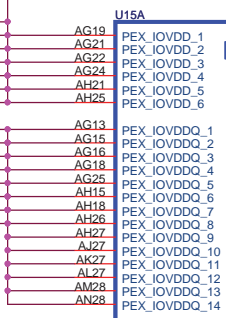
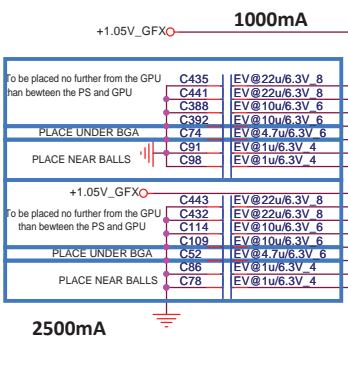


M1 solution

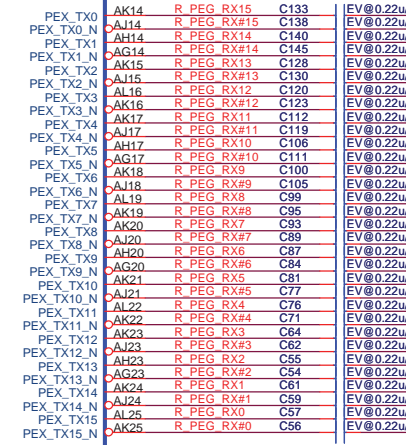
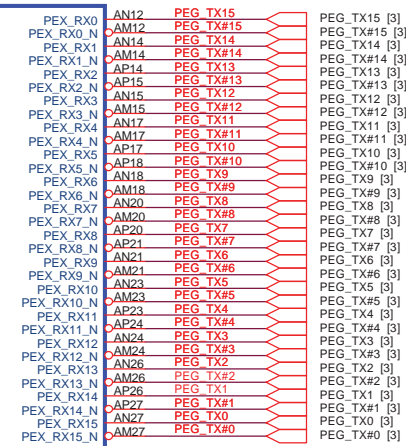


www.vinafix.vn





[PEG Interface]



IV@:iGPU  
EV@dGPU  
OP@:Optimus  
DO@:Discrete only  
SP@:Special

N13P-GL	AJON13P0T02
N13P-GS	AJON13P0T07
N13M-GS	AJON13M0T08

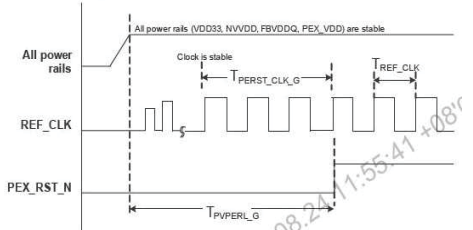
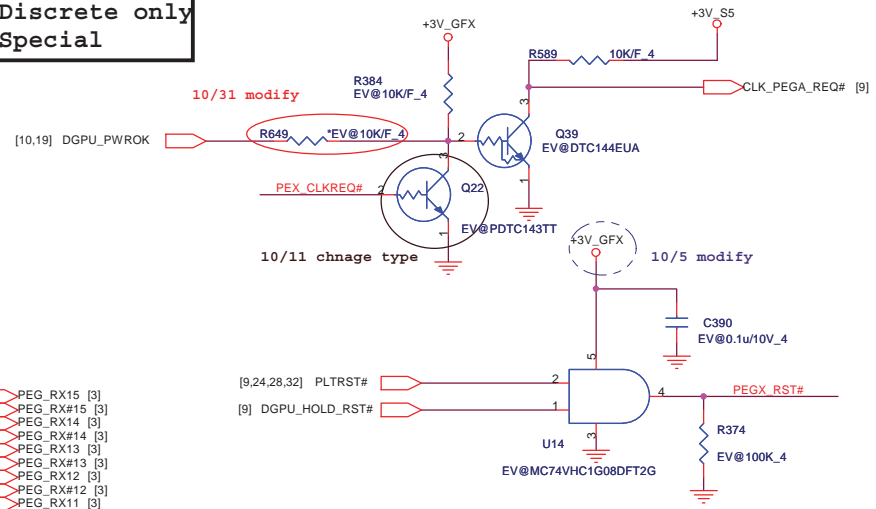
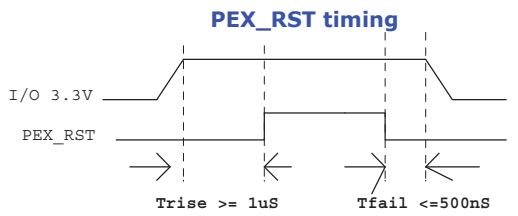


Figure 3-18. PEX\_RST\_N Timing for GPU  
Table 3-8. N11x Reset Requirements for PCI Express 2.0

Constraint Parameter	Requirement	Notes
T <sub>FWPERL_G</sub>	T <sub>FWPERL_G</sub> ≥ 1μs	
T <sub>PERST_CLK_G</sub>	T <sub>PERST_CLK_G</sub> ≥ 1T <sub>REF_CLK</sub>	

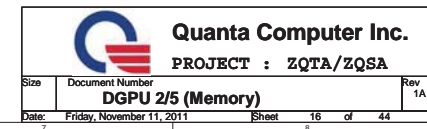
	for N13P/M-GS	for N13P-GL
Stuff--> R	Reserve--> R	
Reserve--> L	Stuff--> L	



**Quanta Computer Inc.**  
**PROJECT : ZQTA/ZQSA**

Size Document Number  
**DGPU 1/5 (PEG)**

Date: Friday, November 11, 2011 Sheet 15 of 44





[15,17,19,39,40] +3V\_GFX

Logical Strap Bit Mapping

	PU-VDD	PD
4.99K	1000	0000
10K	1001	0001
15K	1010	0010
20K	1011	0011
24.9K	1100	0100
30.1K	1101	0101
34.8K	1110	0110
45.3K	1111	0111

N13P-GL	AJ0N13P0T02
N13P-GS	AJ001070T00
N13M-GS	AJ001170T00

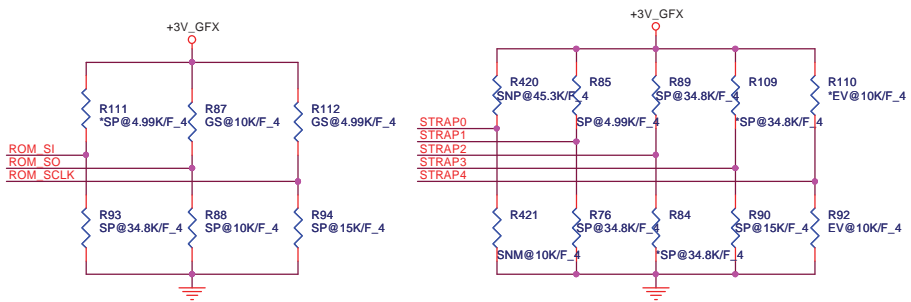
	Logical Strapping Bit3	Logical Strapping Bit2	Logical Strapping Bit1	Logical Strapping Bit0	
ROM_SO	FB_1	FB_0	SMB_ALT_ADDR	VGA_DEVICE	0001
ROM_SCLK	PCI_DEVID[4]	SUB_VENDOR	PCI_DEVID[5]	PEX_PLL_EN_TERM	1010
ROM_SI	RAMCFG[3]	RAMCFG[2]	RAMCFG[1]	RAMCFG[0]	XXXX
STRAP0	USER[3]	USER[2]	USER[1]	USER[0]	1111
STRAP1	3GIO_PADCFG[3]	3GIO_PADCFG[2]	3GIO_PADCFG[1]	3GIO_PADCFG[0]	0110
STRAP2	PCI_DEVID[3]	PCI_DEVID[2]	PCI_DEVID[1]	PCI_DEVID[0]	1110
STRAP3	SOR3_EXPOSED	SOR2_EXPOSED	SOR1_EXPOSED	SOR0_EXPOSED	0010
STRAP4	RESERVED	PCI SPEED CHANGE GEN3	PCI_MAX SPEED	DP_PLL_VDD33	0011

**STRAP2**  
N13P-GL (1001) --> 10k PU  
N13P-GS (1011) --> 20K PU

**STRAP1**  
N13P-GL (0111) --> 45.3k PD  
N13P-GS (0110) --> 34.8K PD

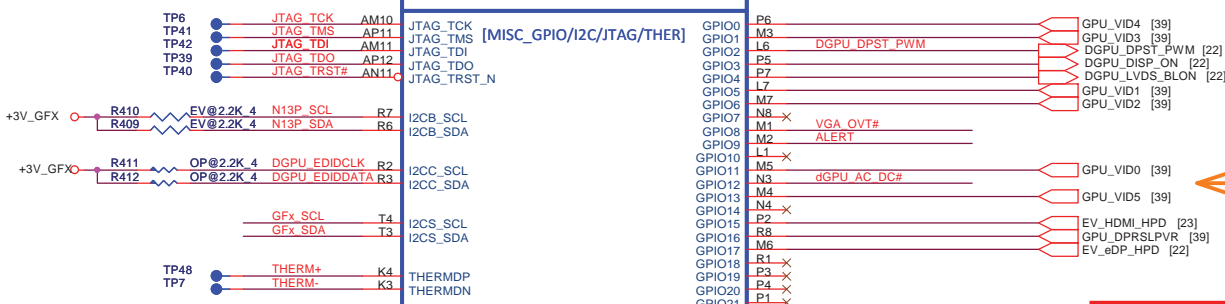
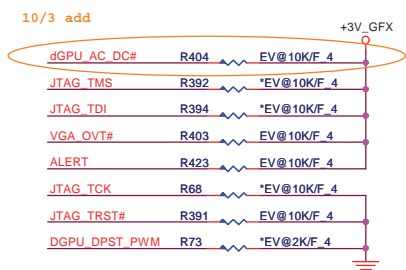
**STRAP3**  
Optimus --> 4.99k PD  
Discrete only --> 15K PD

**Resistor P/N**  
4.99K--> CS24992FB26  
10K --> CS31002FB26  
15K --> CS31502FB24  
20K --> CS32002FB29  
34.8K--> CS33482FB22  
45.3K --> CS34532FB18

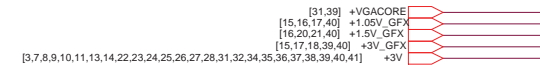


N13P-GS/-GL Strapping table

ROM_SI	1G Hynix 64Mx16 -->15K PD 1G Micron 64Mx16 -->20K PD 2G Hynix 128Mx16 -->35K PD (Default) 2G Micron 128Mx16 -->45K PD	ROM_SO N13P-GL --> 10K PD N13P-GS --> 10K PU	ROM_SCLK N13P-GL (0010) --> 15k PD N13P-GS (1000) --> 4.99K PU
--------	--	--	--

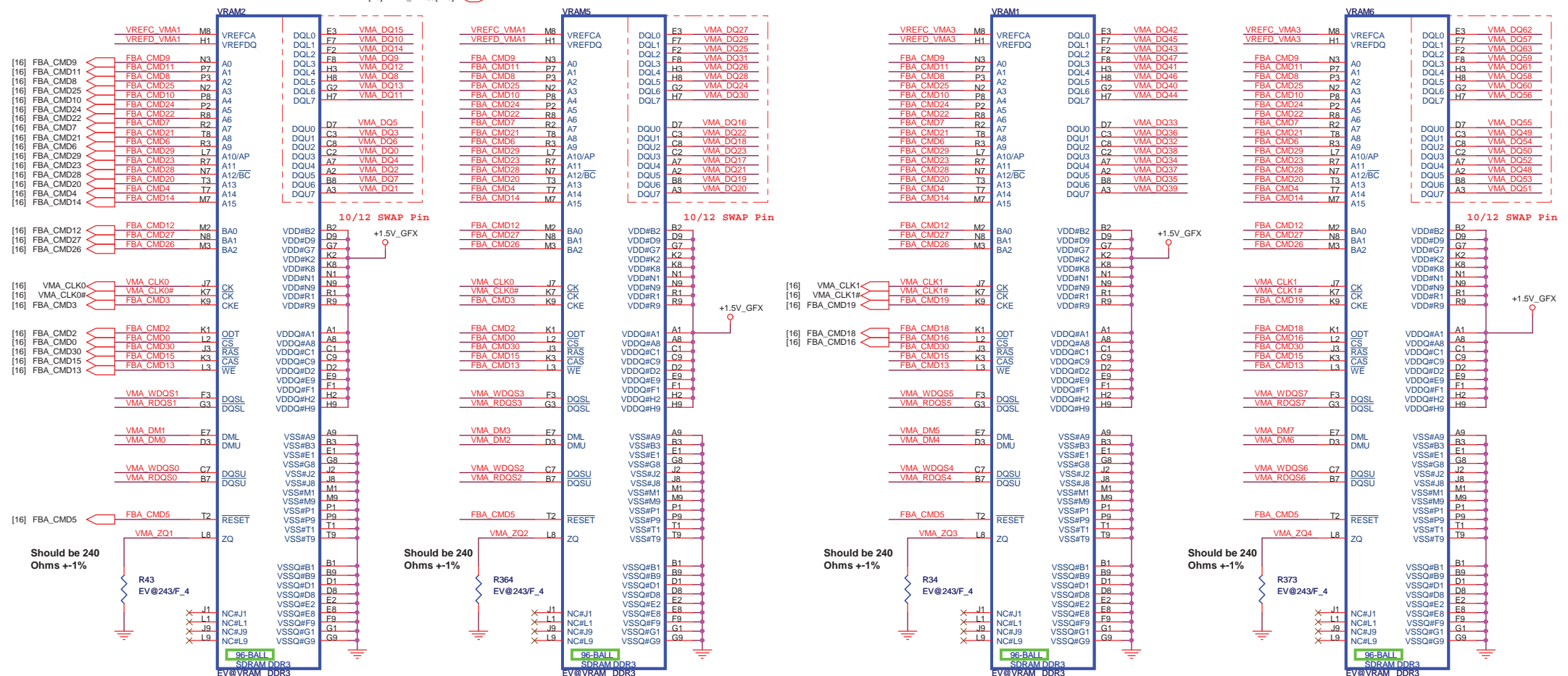




3

[16] VMA\_DQ[63..0]  
[16] VMA\_DM[7..0]  
[16] VMA\_WDQS[7..0]  
[16] VMA\_RDQS[7..0]

# CHANNEL A: 256MB/512MB DDR3



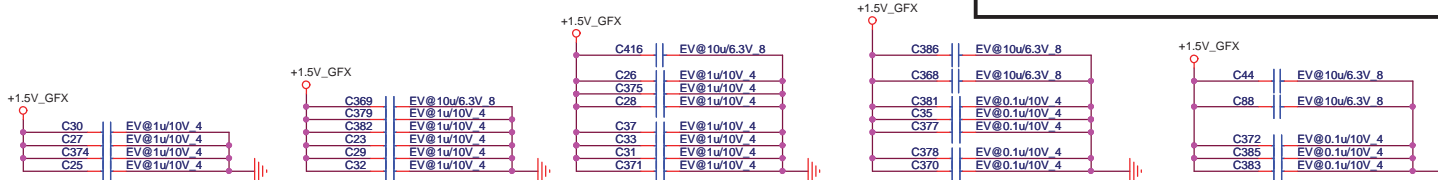
VMA\_CLK0  
R371 EV@162/F\_4  
VMA\_CLK0#

Fermi : Change to 160 ohm  
1 : CS11602JB00 ,RES CHIP 160 1/16W +-5% (0402)  
2 : CS11622PB07 ,RES CHIP 162 1/16W +-1% (0402)

[16] FBA\_CMD17 FBA\_CMD17 TP1  
[16] FBA\_CMD1 FBA\_CMD1 TP2  
10/14 modify

VMA\_CLK1  
R41 EV@162/F\_4  
VMA\_CLK1#

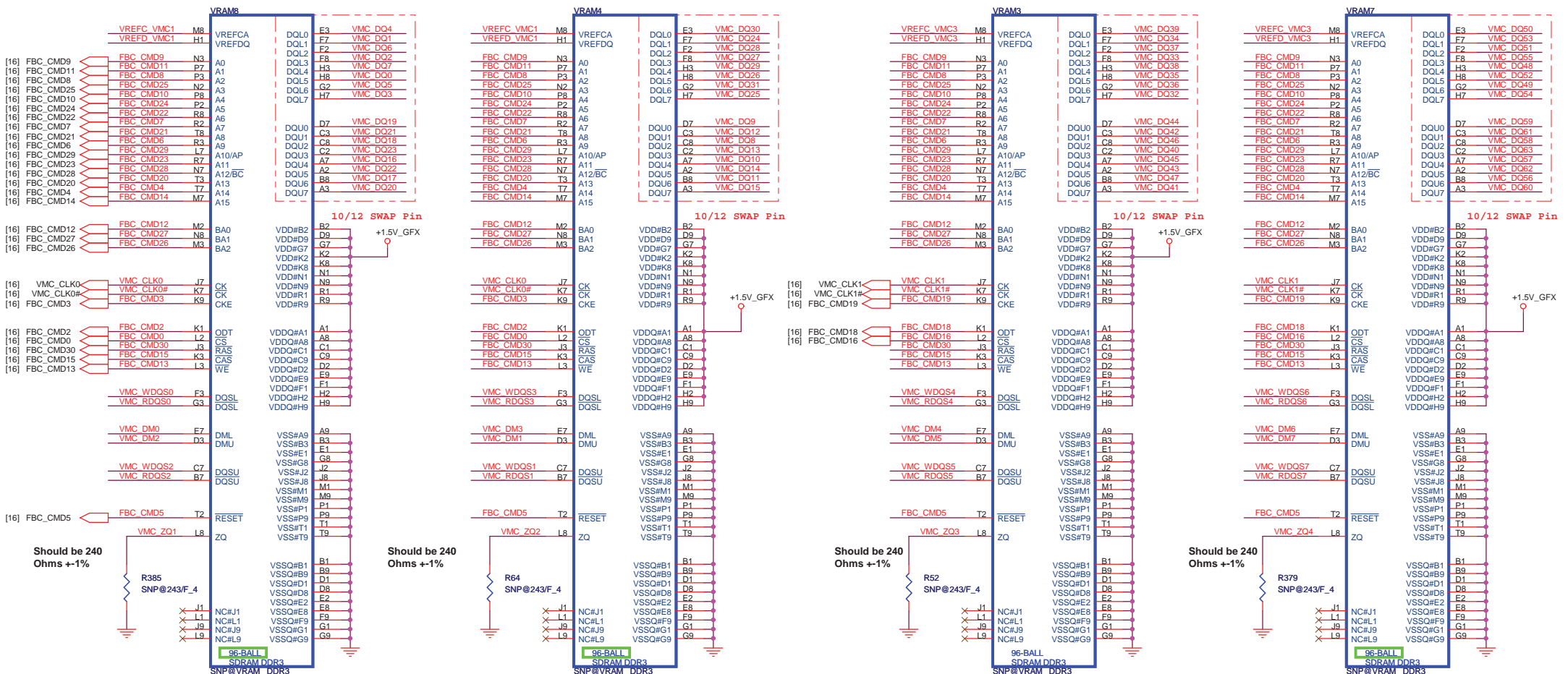
Fermi : Change to 160 ohm  
1 : CS11602JB00 ,RES CHIP 160 1/16W +-5% (0402)  
2 : CS11622PB07 ,RES CHIP 162 1/16W +-1% (0402)





[16] VMC\_DQ[63..0]  
[16] VMC\_DM[7..0]  
[16] VMC\_WDQS[7..0]  
[16] VMC\_RDQS[7..0]

# CHANNEL B: 256MB/512MB DDR3

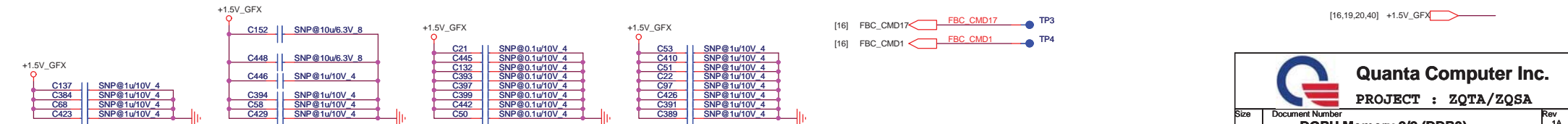


VMC\_CLK0  
R388 SNP@162/F\_4  
VMC\_CLK0#

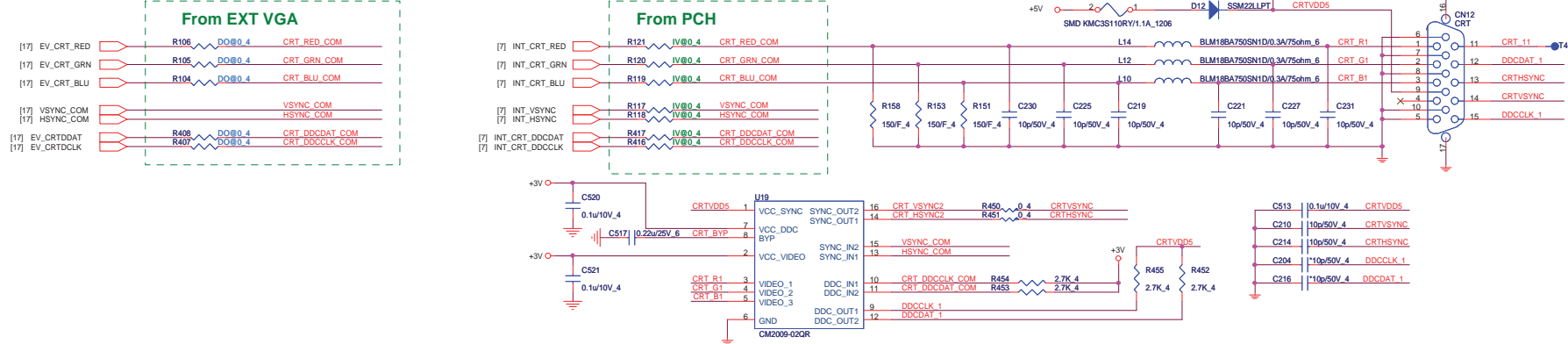
Fermi : Change to 160 ohm  
1 : CS11602JB00 ,RES CHIP 160 1/16W +5% (0402)  
2 : CS11622PB07 ,RES CHIP 162 1/16W +-1% (0402)

VMC\_CLK1  
R49 SNP@162/F\_4  
VMC\_CLK1#

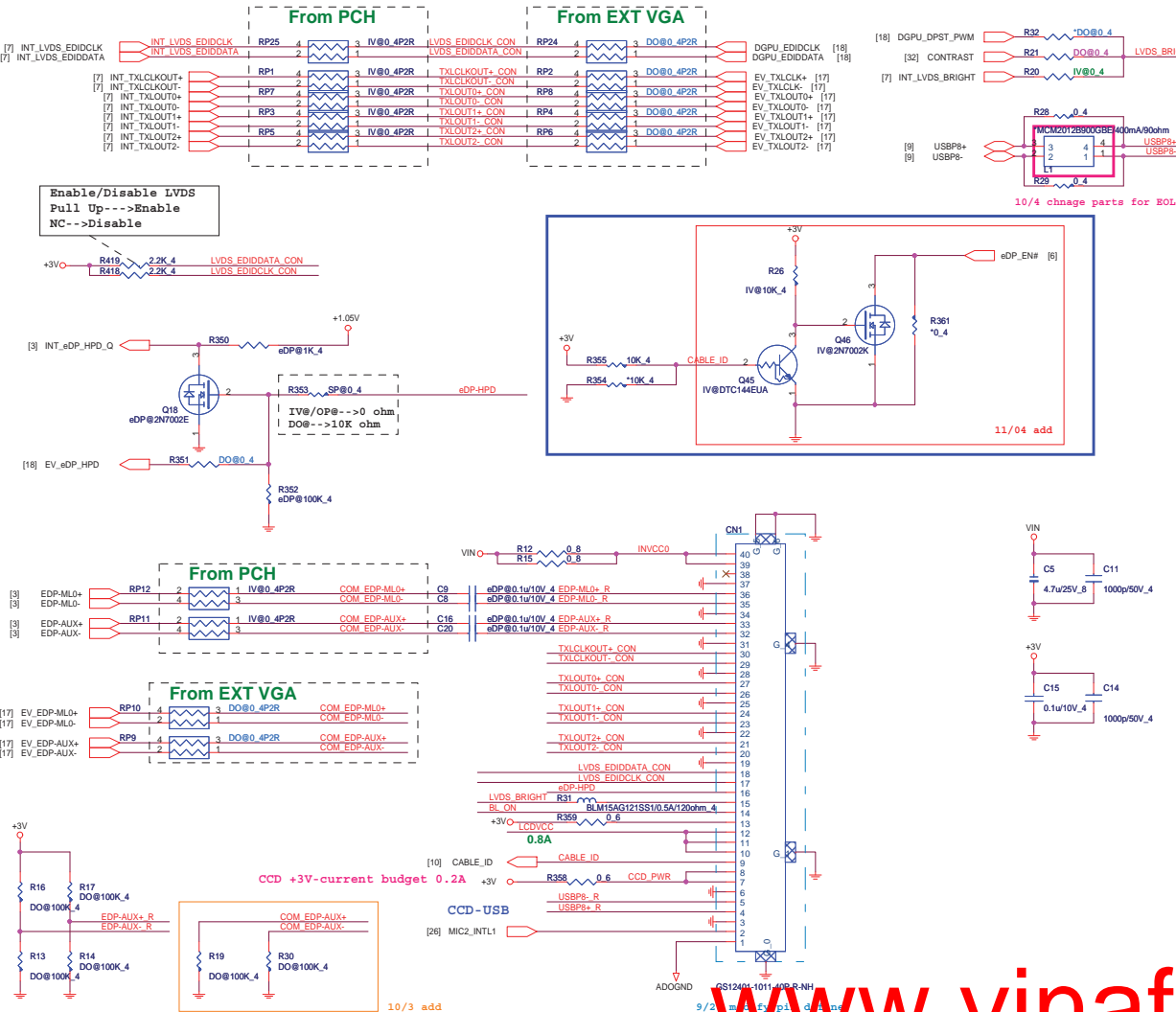
Fermi : Change to 160 ohm  
1 : CS11602JB00 ,RES CHIP 160 1/16W +5% (0402)  
2 : CS11622PB07 ,RES CHIP 162 1/16W +-1% (0402)



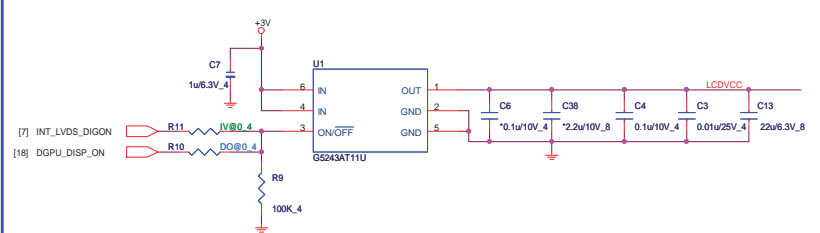
## CRT



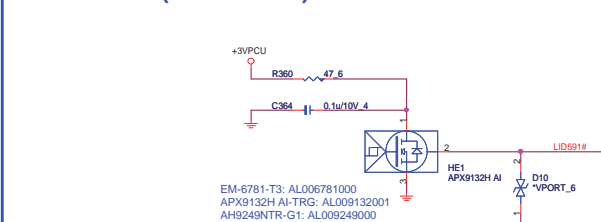
## LVDS & eDP



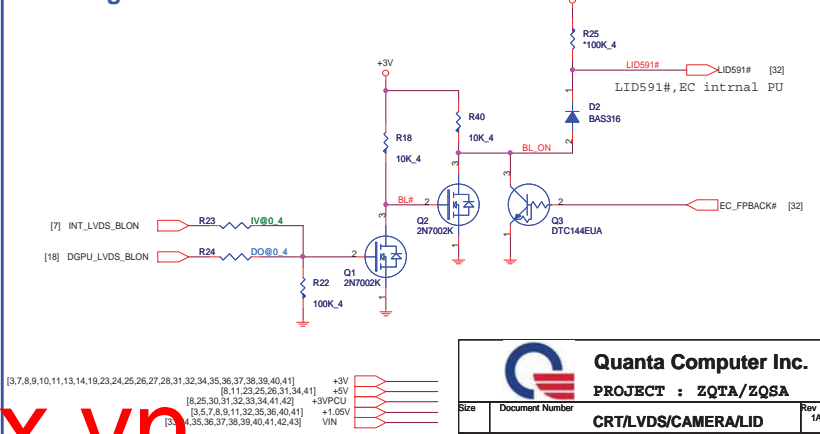
## LCD Power



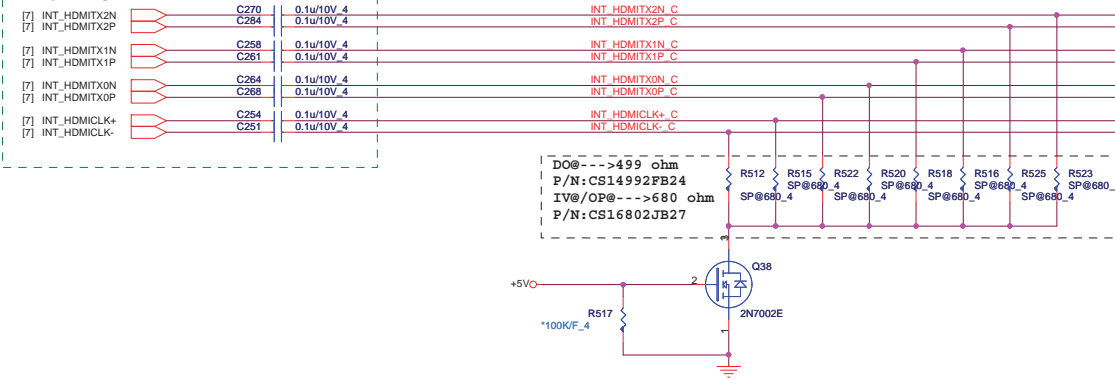
## Lid Switch (Hall sensor)



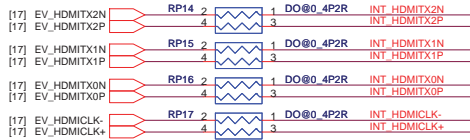
## Backlight Control



## From PCH

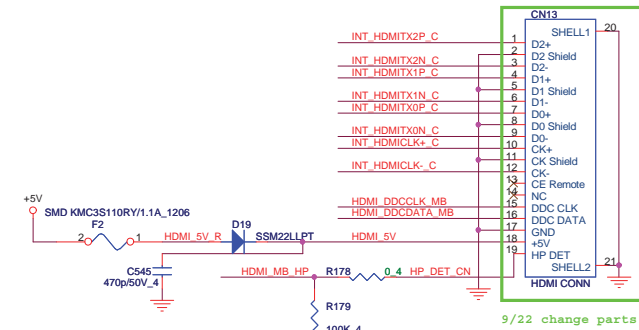


## From EXT VGA

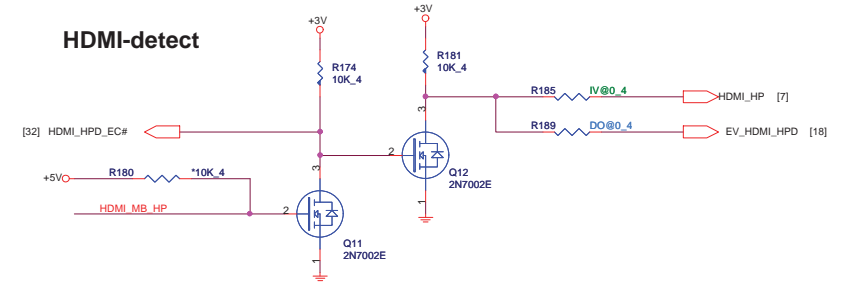


IV@:iGPU  
EV@:dGPU  
OP@:Optimus  
DO@:Discrete only  
SP@:Special

## HDMI connector



## HDMI-detect



## I2C

UMA	R239	CS22202JB18
	R245	
DIS	R239	CS24702JB38
	R245	

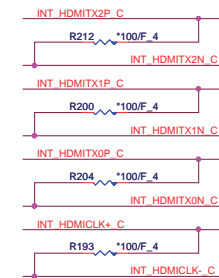
## From EXT VGA



## From PCH

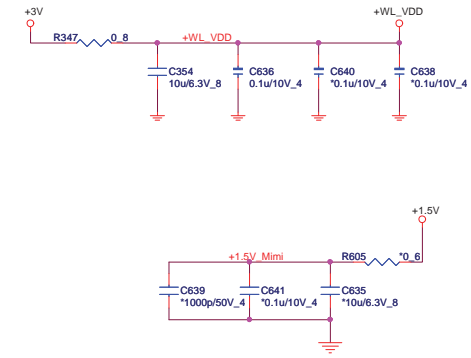
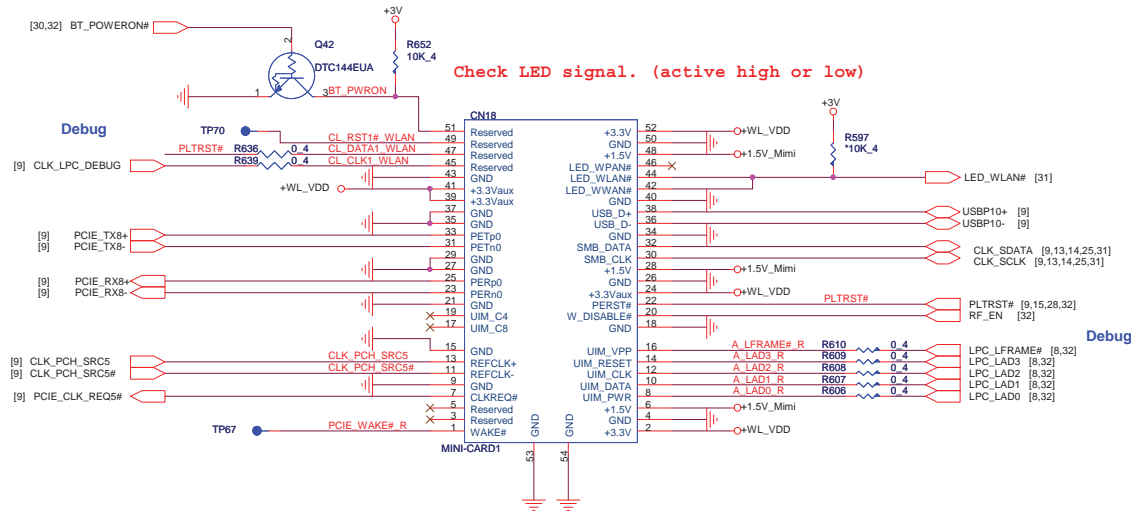


## EMI

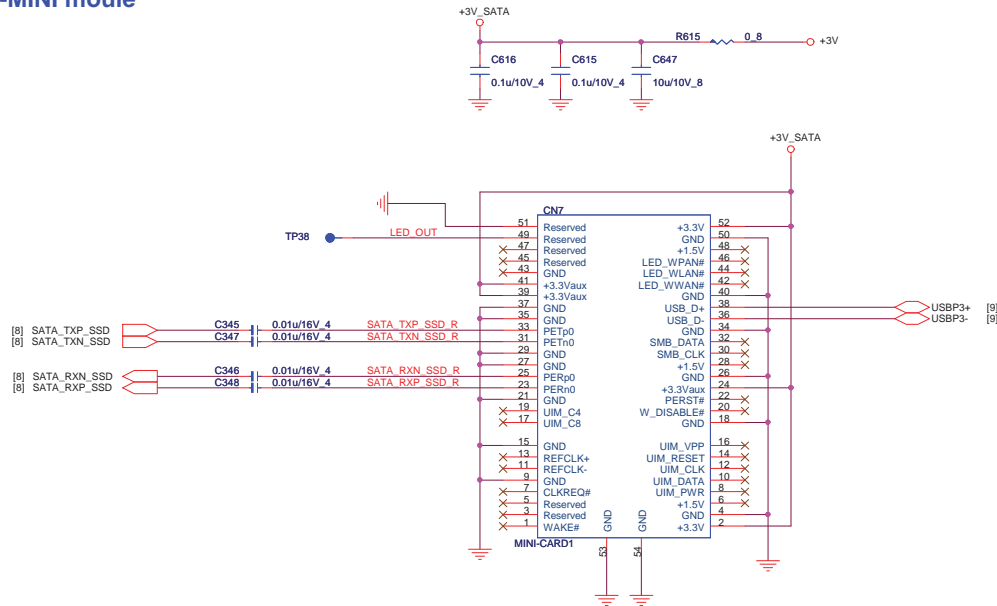


## MINI-CARD WLAN(MPC)

+3.3V: 1000mA  
+3.3Vaux:330mA  
+1.5V:500mA

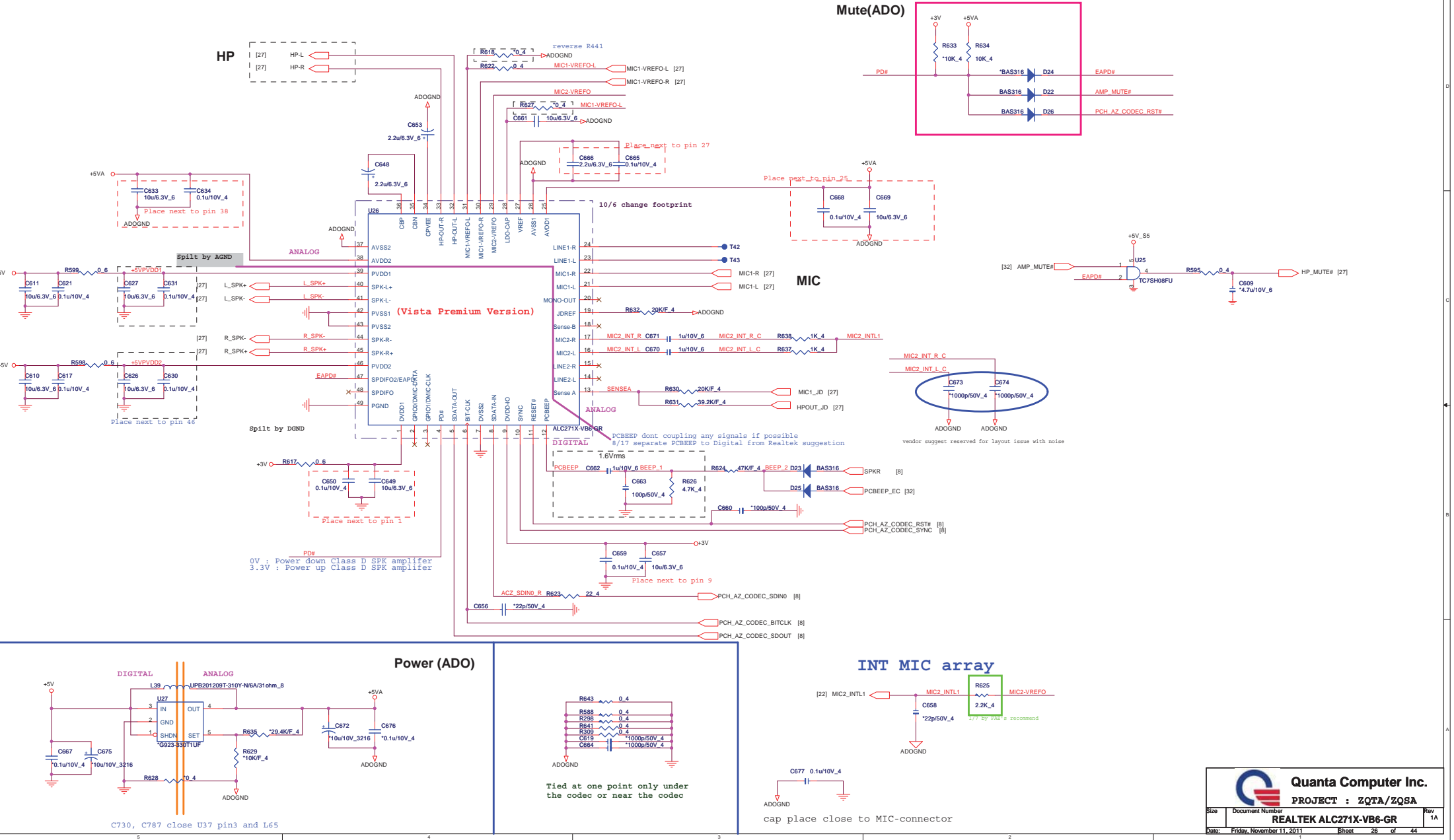


## SSD-MINI moule





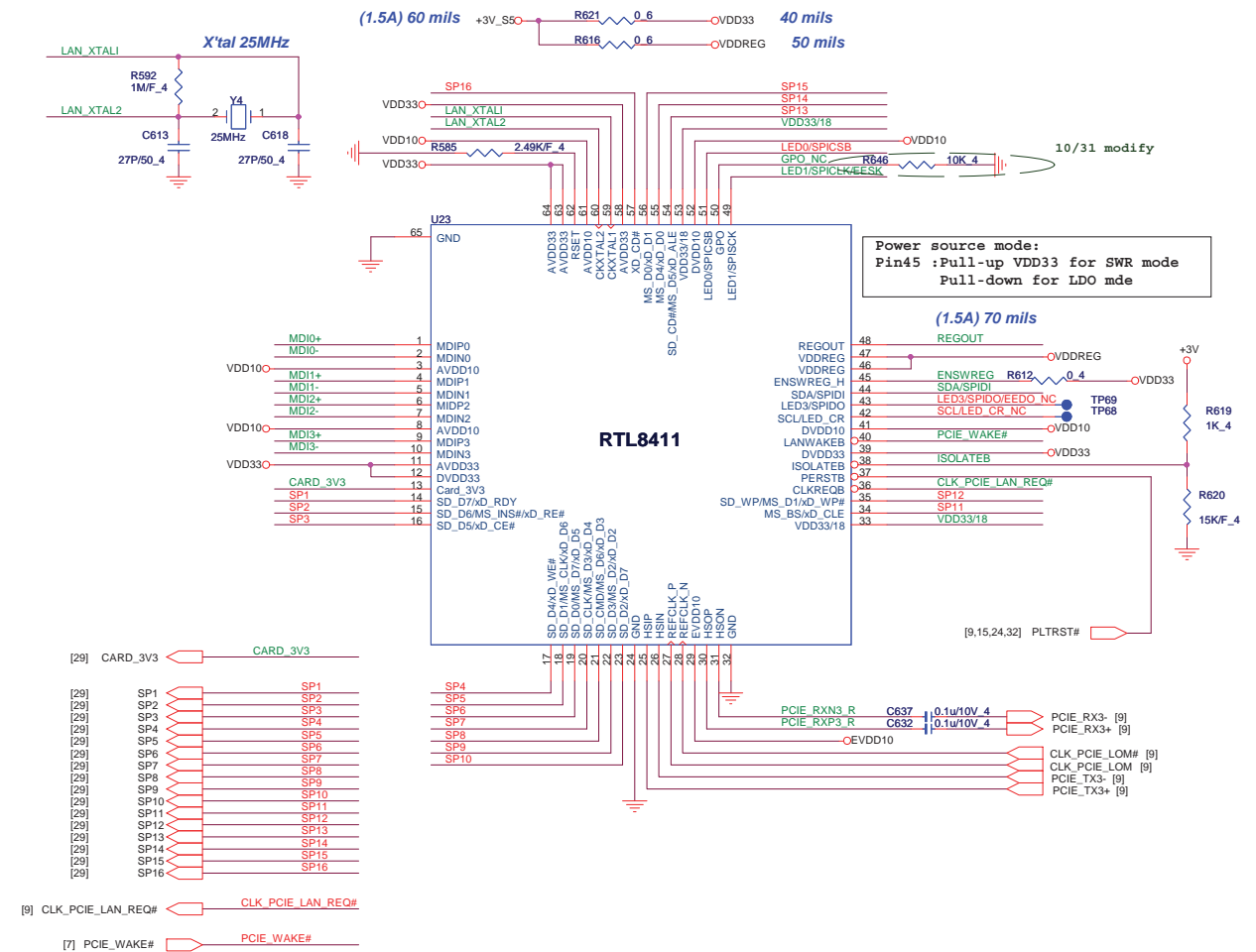
Codec(ADO)



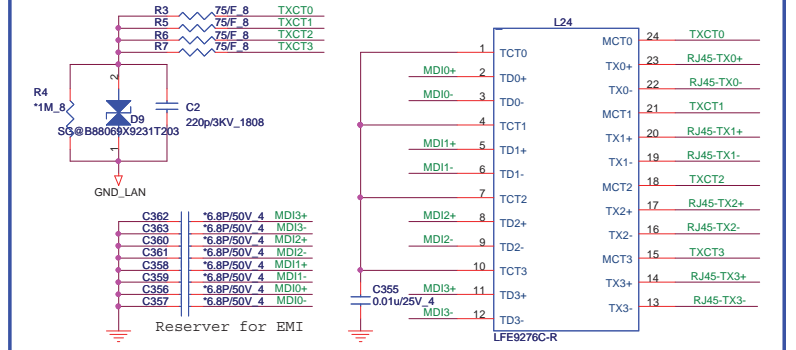




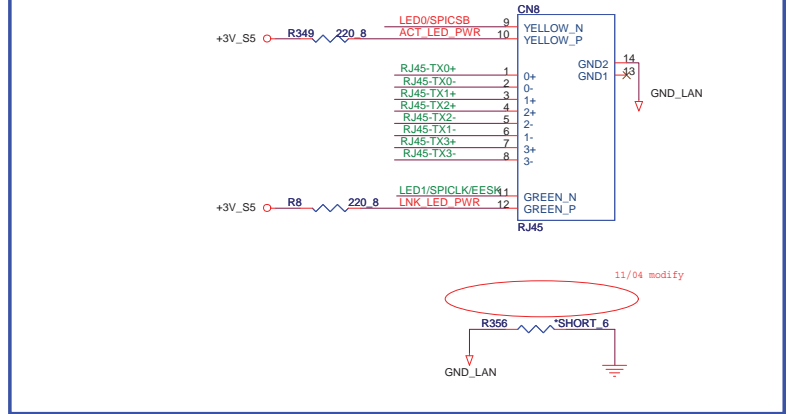
# LAN/Card reader



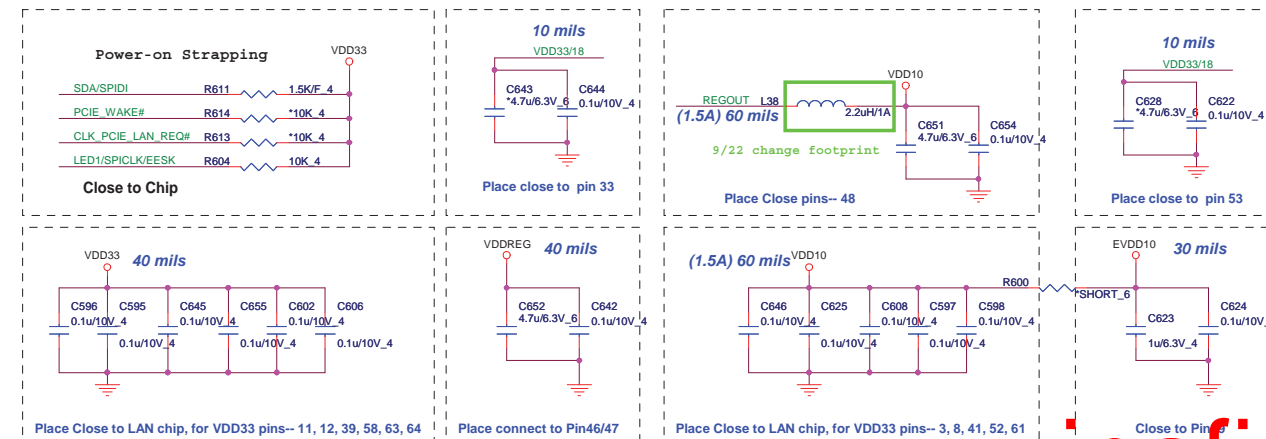
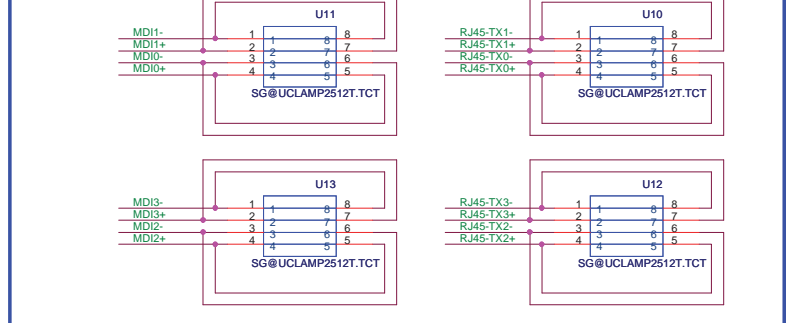
## Transformer



## RJ45



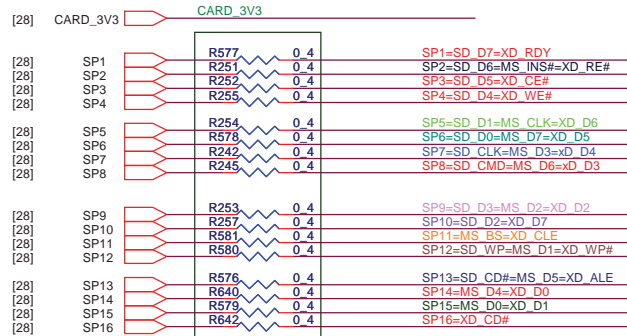
## SURGE



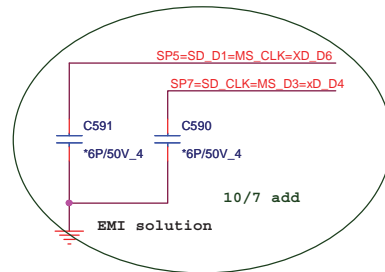
# CARD READER CONNECTOR

## Share Pin

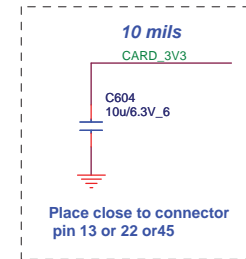
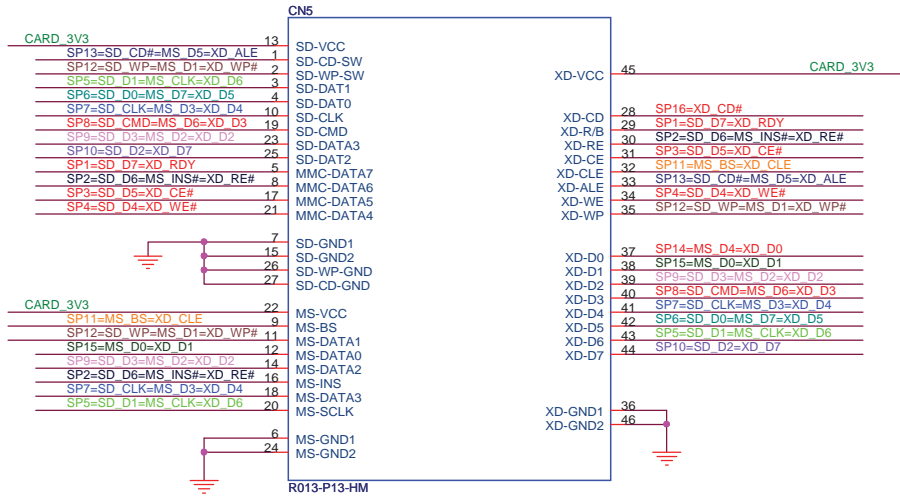
SP1	SD_D7		xD_RDY
SP2	SD_D6	MS_INS#	xD_RE#
SP3	SD_D5		xD_CE#
SP4	SD_D4		xD_WE#
SP5	SD_D1	MS_CLK	xD_D6
SP6	SD_D0	MS_D7	xD_D5
SP7	SD_CLK	MS_D3	xD_D4
SP8	SD_CMD	MS_D6	xD_D3
SP9	SD_D3	MS_D2	xD_D2
SP10	SD_D2		xD_D7
SP11		MS_BS	xD_CLE
SP12	SD_WP	MS_D1	xD_WP#
SP13	SD_CD#	MS_D5	xD_ALE
SP14		MS_D4	xD_D0
SP15		MS_D0	xD_D1
SP16			xD_CD#



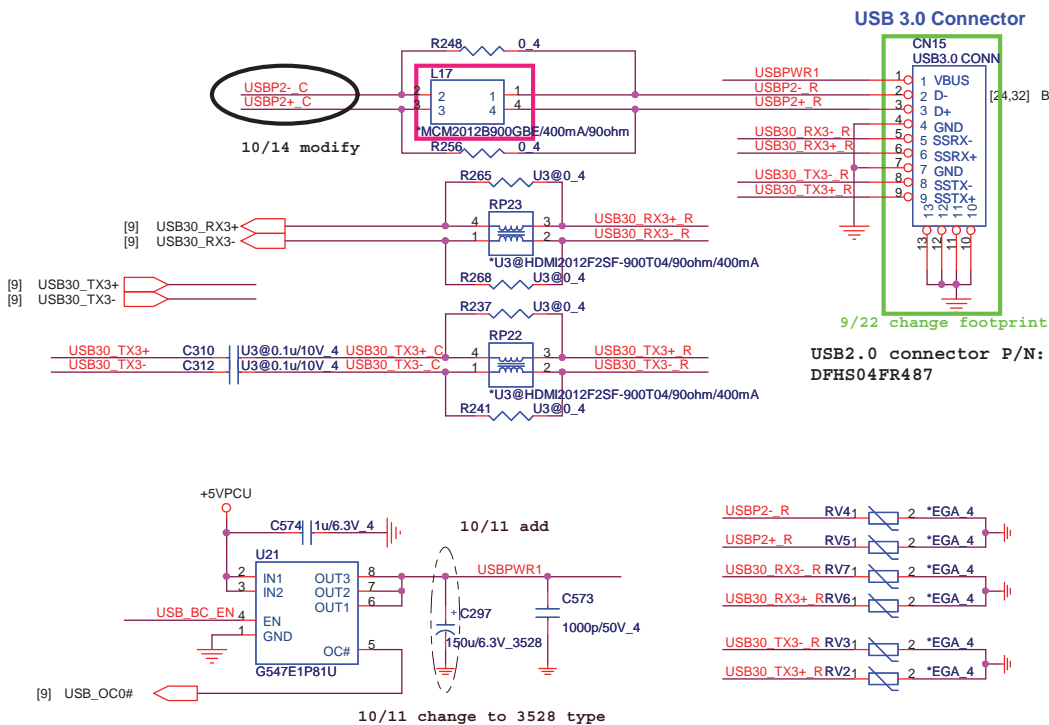
10/7 change 0 ohm



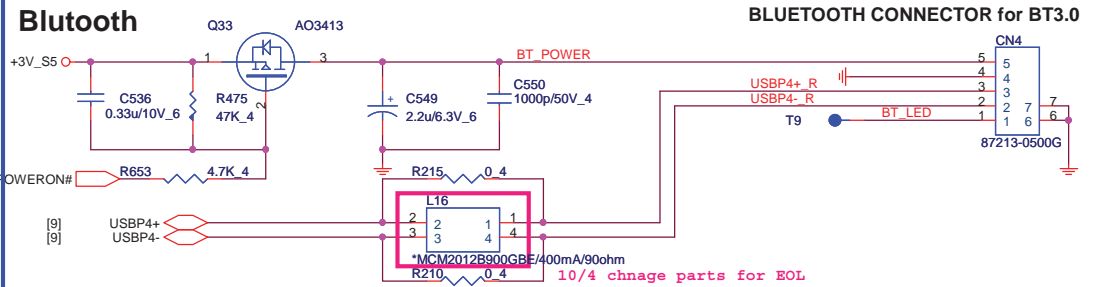
# XD,MMC 4.2/SD,MS/MSP 7 IN1 CARD READER



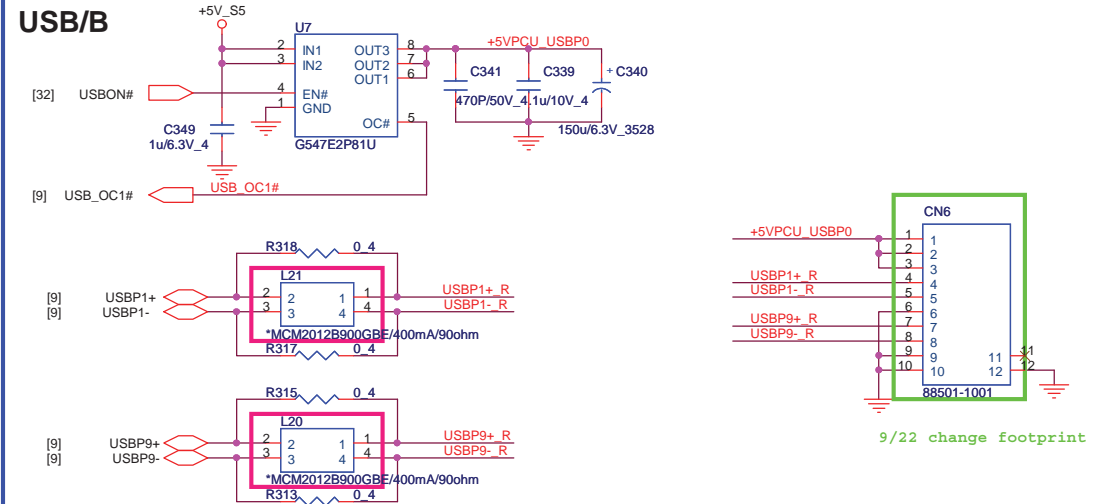
## USB3.0/2.0



## Bluetooth

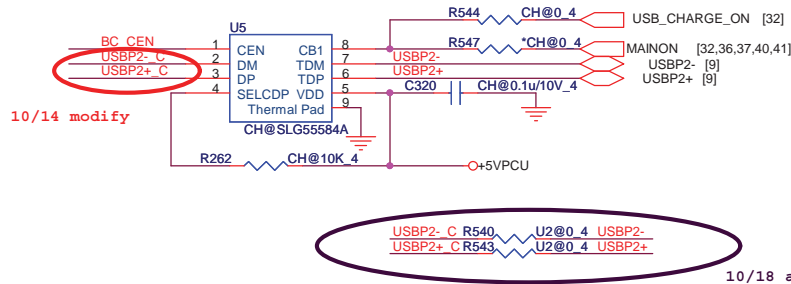


## USB/B

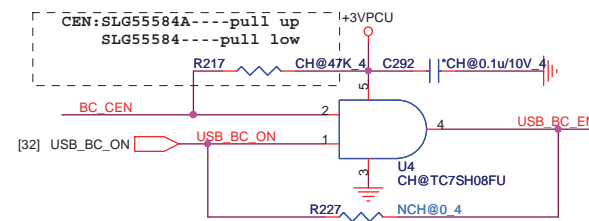


## USB Charger to 3.0

CB	SELCDP	Function
0	X	DCP autodetect with mouse/keyboard wakeup
1	0	S0 charging with SDP only
1	1	S0 charging with CDP or SDP only (depending on external device)



USB Charger -->CH@  
None Charger--> NCH@

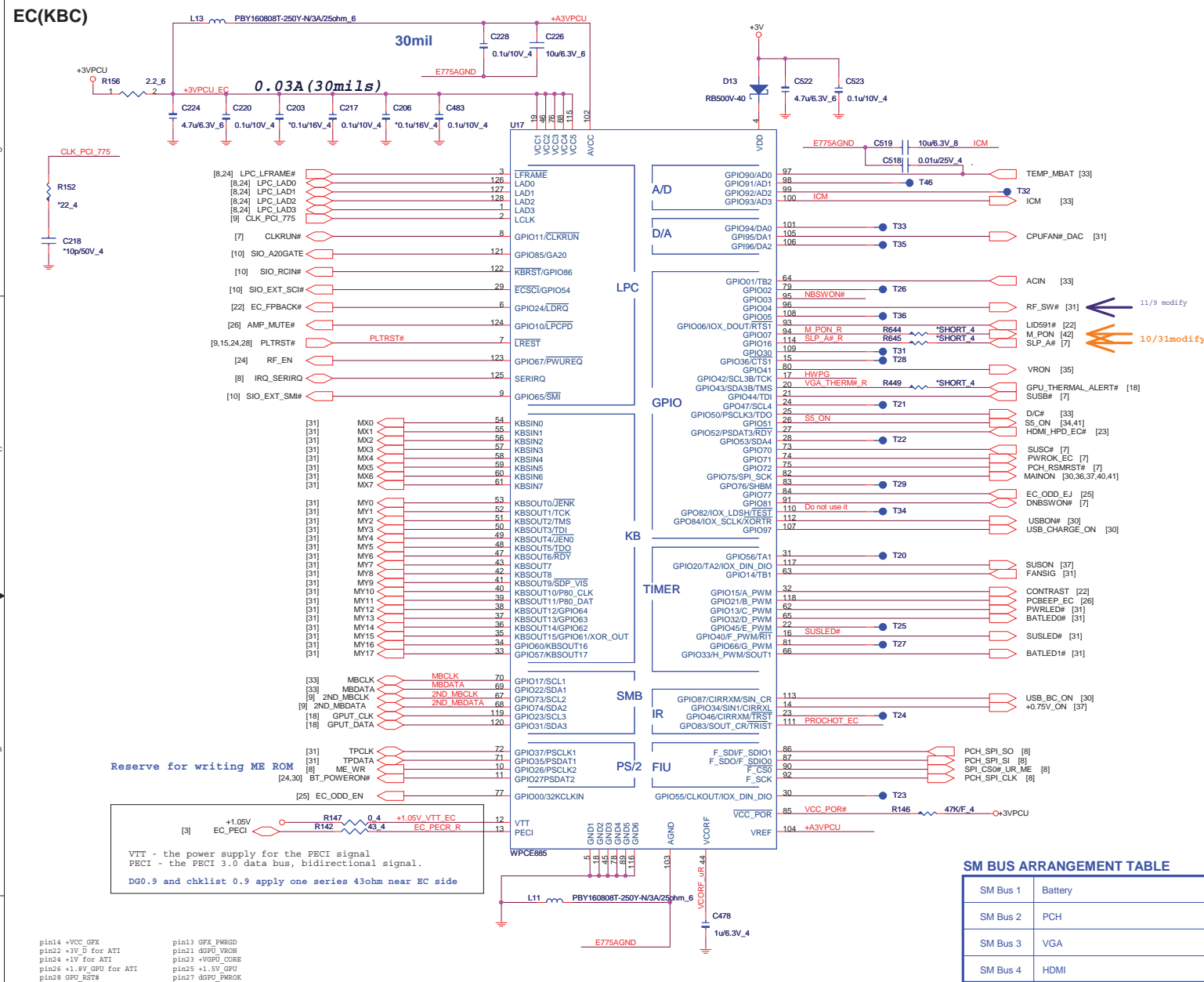


Quanta Computer Inc.  
PROJECT : ZQTA/ZQSA

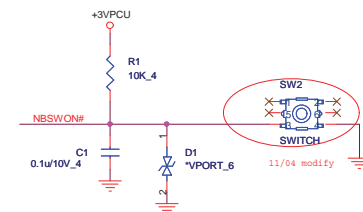
Size	Document Number	Rev
1A	USB/ BT/CHARGER	1A
Date:	Friday, November 11, 2011	Sheet 30 of 44



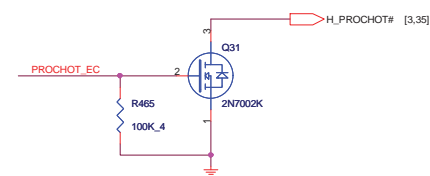
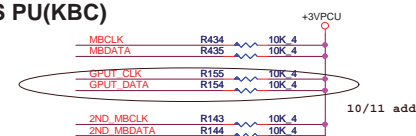
**EC(KBC)**



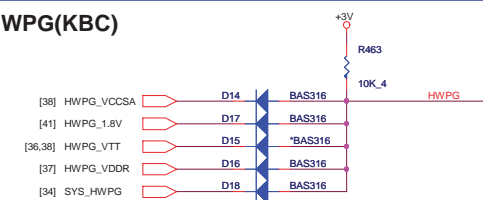
## Power on bottom



## SM BUS PU(KBC)

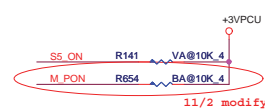


## HWPG(KBC)



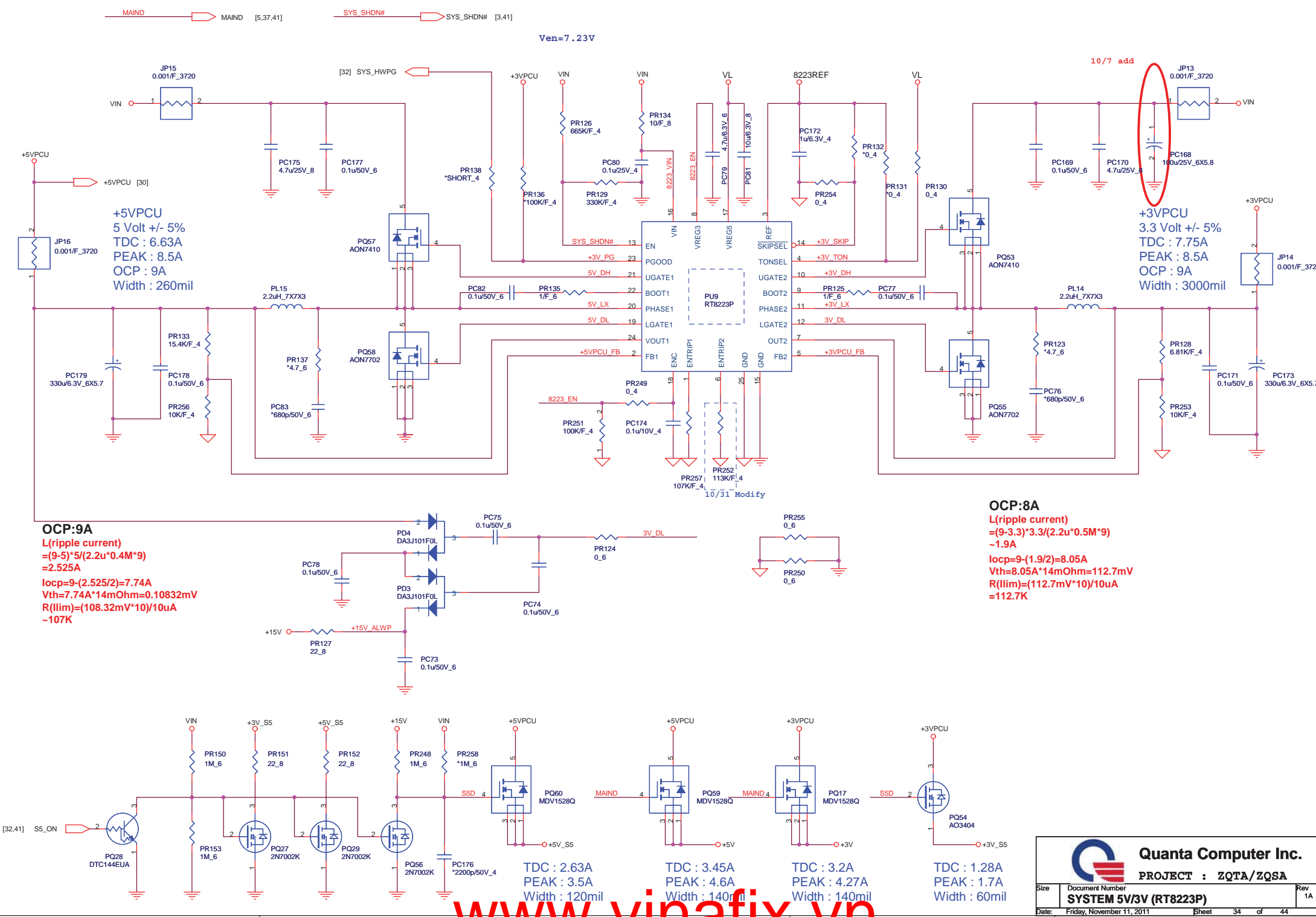
### SM BUS ARRANGEMENT TABLE

SM Bus 1	Battery
SM Bus 2	PCH
SM Bus 3	VGA
SM Bus 4	HDMI









**OCP:9A**  
L(ripple current)  
=(9-5)\*5/(2.2u\*0.4M\*9)  
=2.525A  
Iocp=9-(2.525/2)=7.74A  
Vth=7.74A\*14mOhm=0.10832mV  
R(Ilim)=(108.32mV\*10)/10uA  
~107K

**OCP:8A**  
L(ripple current)  
=(9-3.3)\*3.3/(2.2u\*0.5M\*9)  
~1.9A  
Iocp=9-(1.9/2)=8.05A  
Vth=8.05A\*14mOhm=112.7mV  
R(Ilim)=(112.7mV\*10)/10uA  
=112.7K

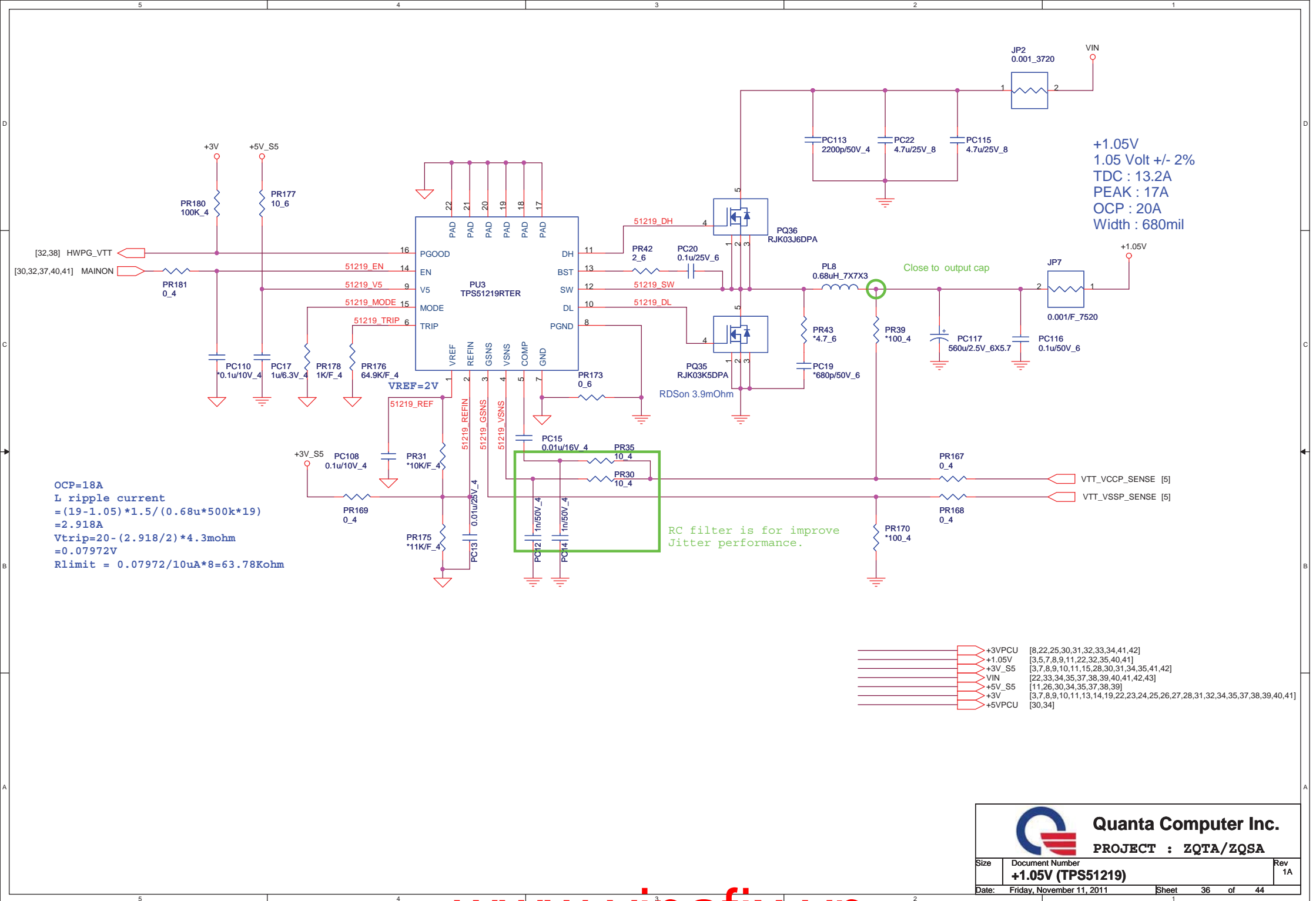
TDC : 2.63A  
PEAK : 3.5A  
Width : 120mil

TDC : 3.45A  
PEAK : 4.6A  
Width : 140mil

TDC : 3.2A  
PEAK : 4.27A  
Width : 140mil

TDC : 1.28A  
PEAK : 1.7A  
Width : 60mil

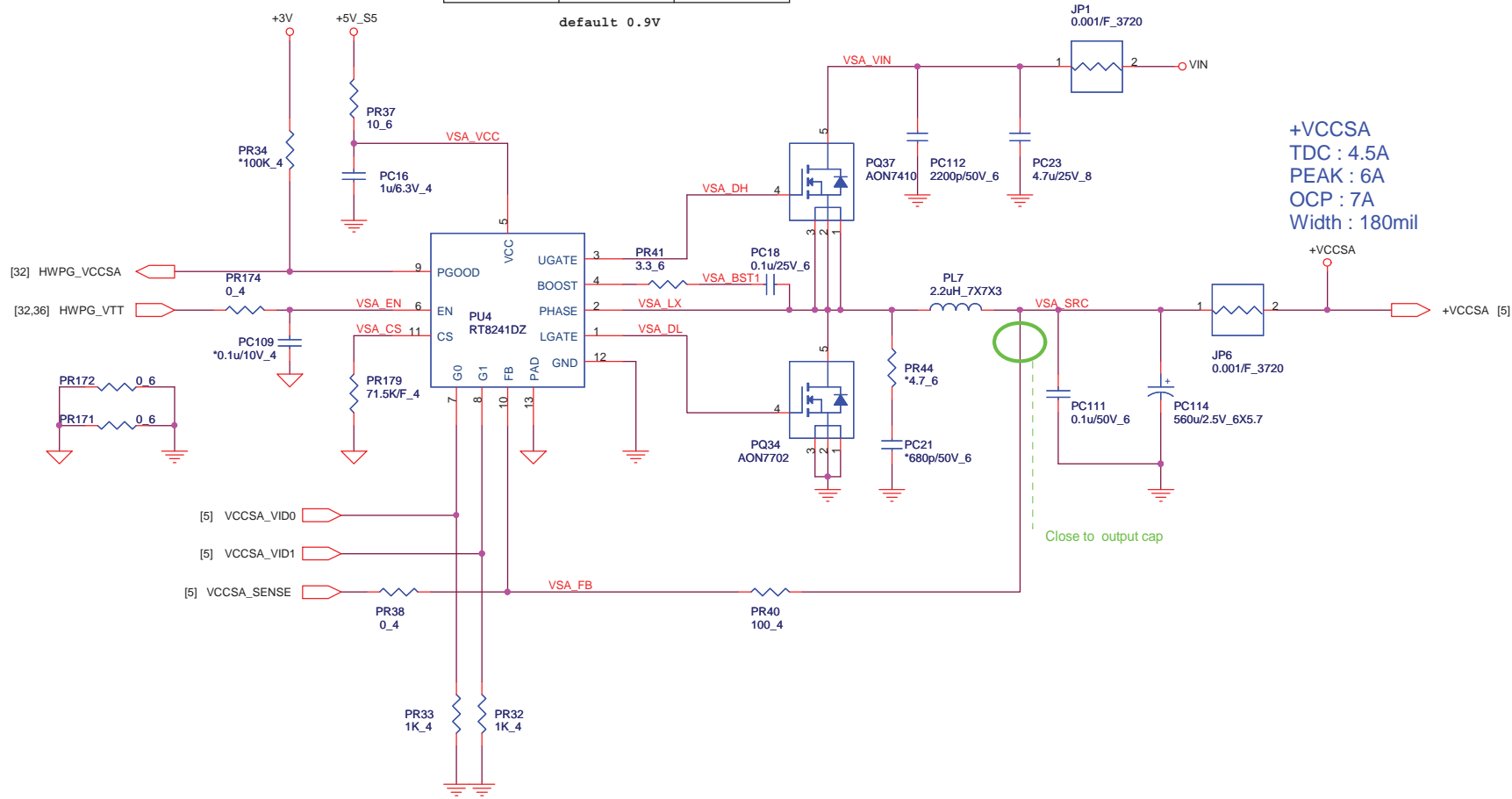






G0	G1	+VCCSA
0	0	0.9V
0	1	0.8V
1	0	0.725V
1	1	0.675V

default 0.9V



+VCCSA  
TDC : 4.5A  
PEAK : 6A  
OCP : 7A  
Width : 180mil

Close to output cap

OCP=7A  
Iripple=(19-0.9)\*0.9/(2.2u\*300K\*19)  
=1.299A  
Rth=14mohm\*8\*(7-0.65)/10uA  
=71.125K  
Ipeak=8.299A



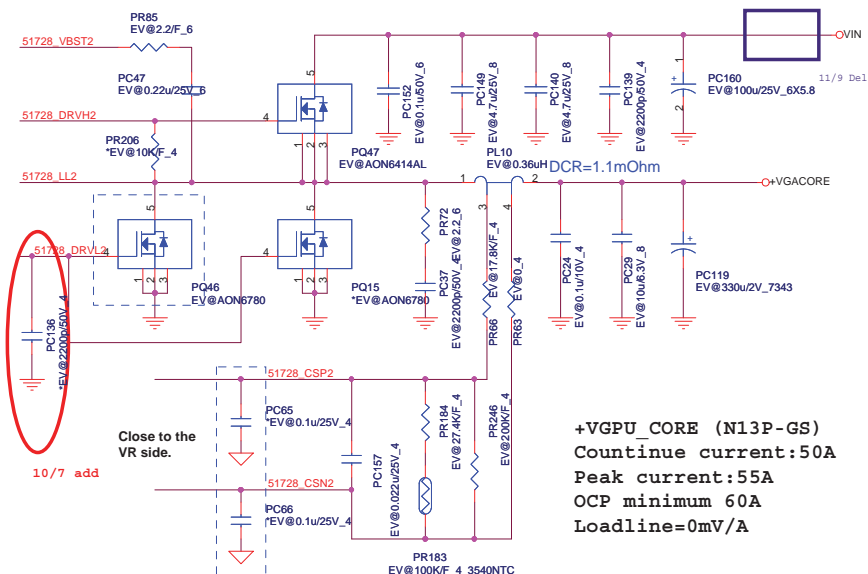
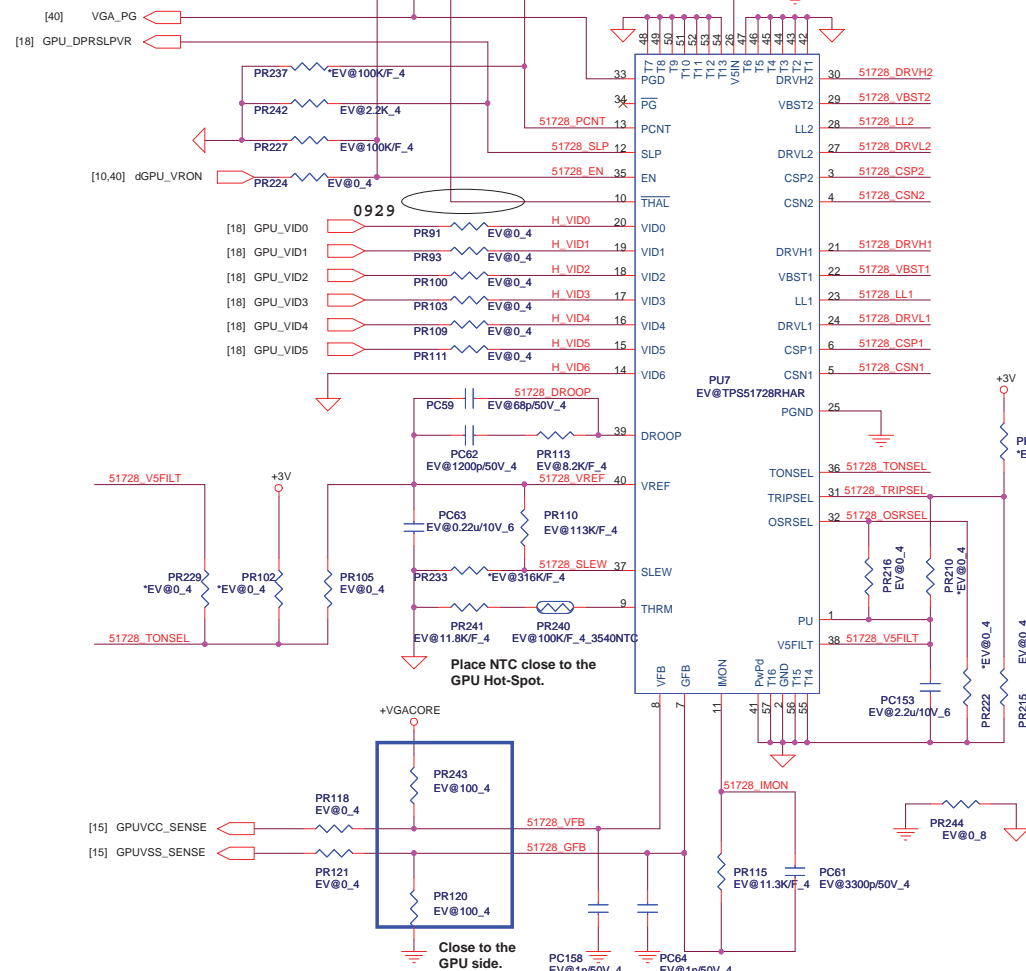
**Quanta Computer Inc.**  
**PROJECT : ZQTA/ZQSA**

Size	Document Number	Rev
	<b>VCCSA(RT8241DZ)</b>	1A
Date:	Friday, November 11, 2011	Sheet 38 of 44

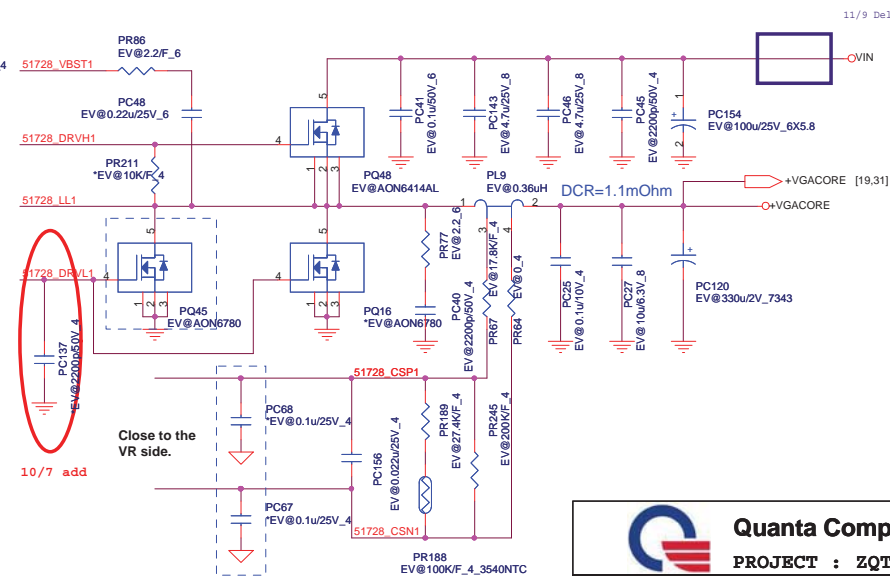


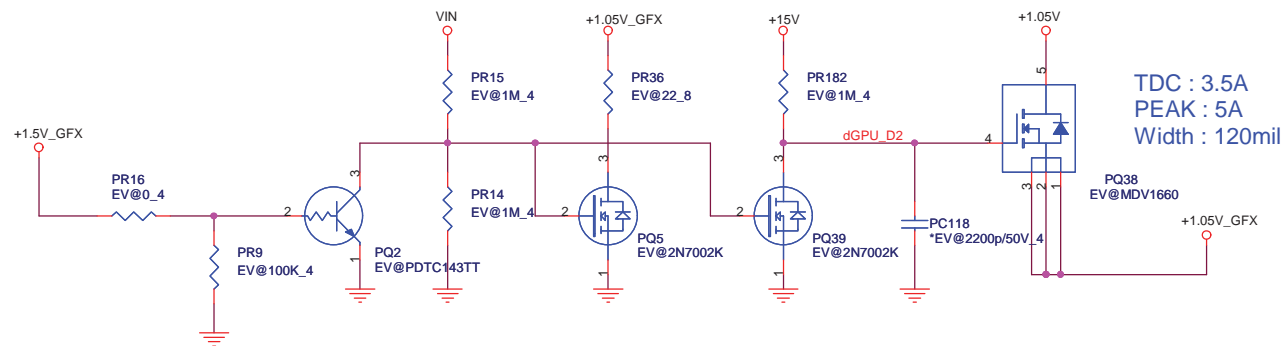
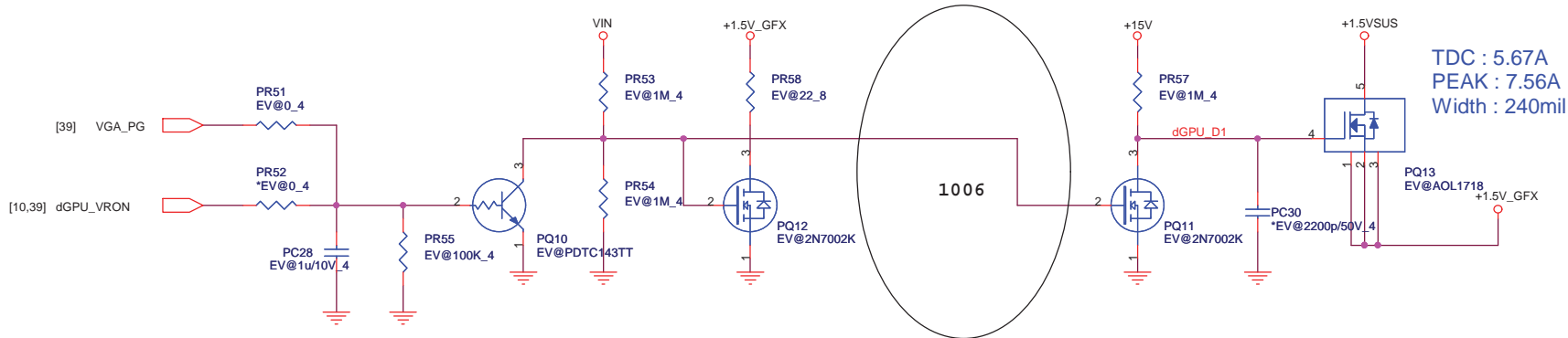
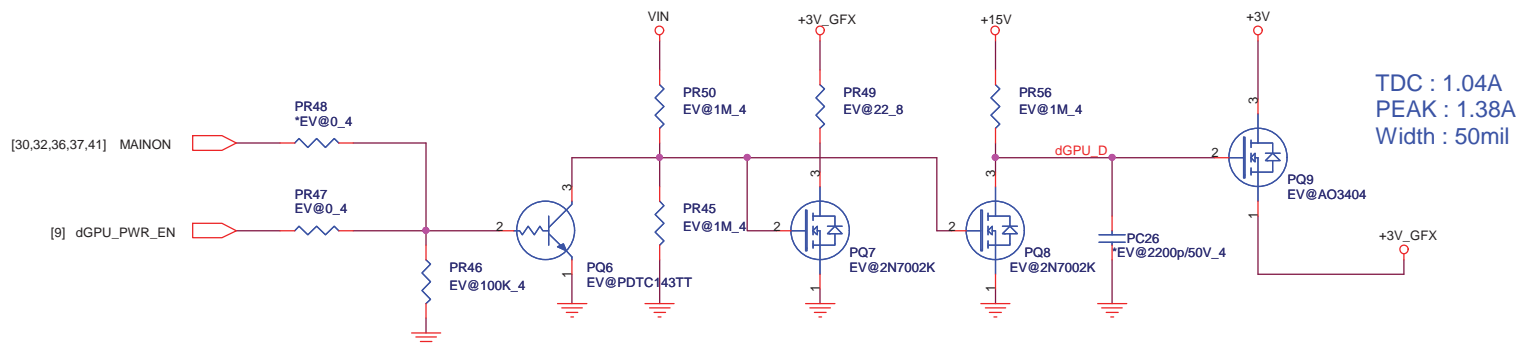
1013

	VID5	VID4	VID3	VID2	VID1	VID0
N13P-GL QS	1	0	1	1	0	0
N13P-GS QS N13M-GS ES	1	1	0	0	0	0



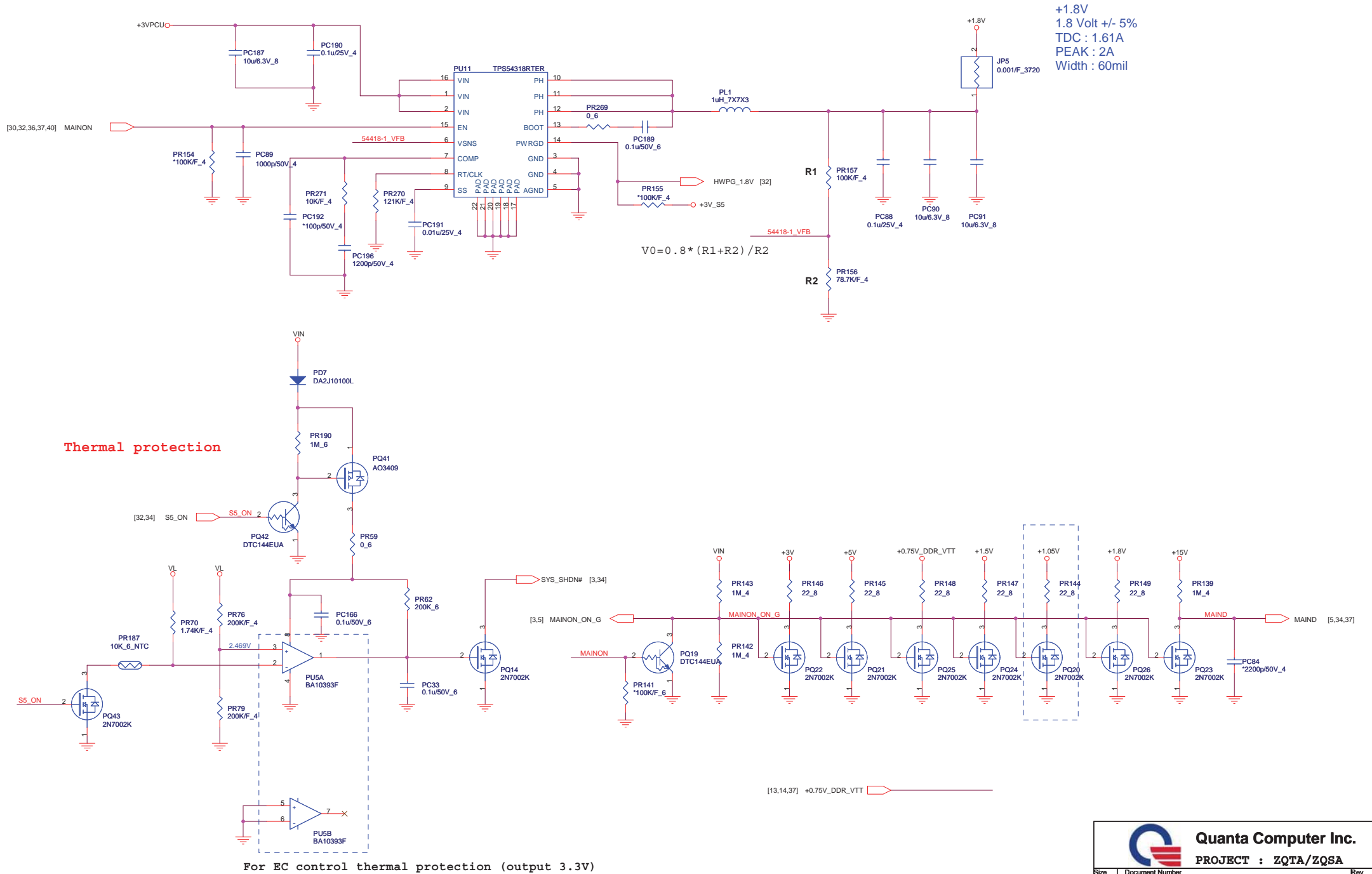
```
+VGPU_CORE (N13P-GS)
Continue current:50A
Peak current:55A
OCP minimum 60A
Loadline=0mV/A
```

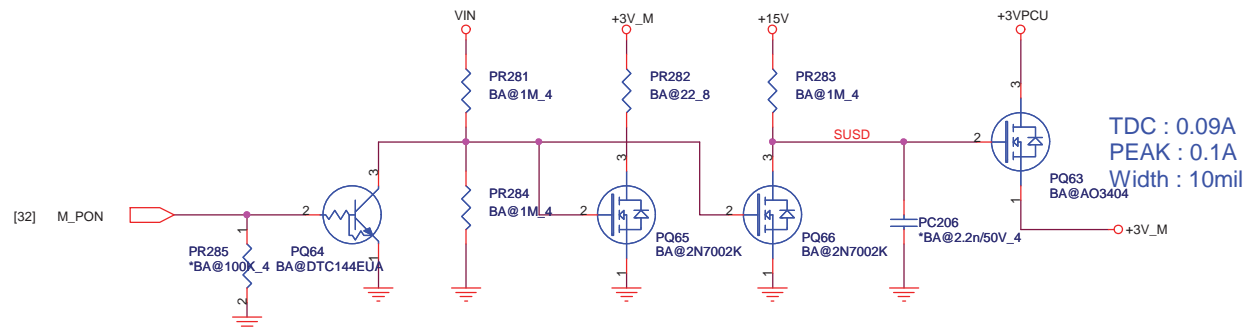
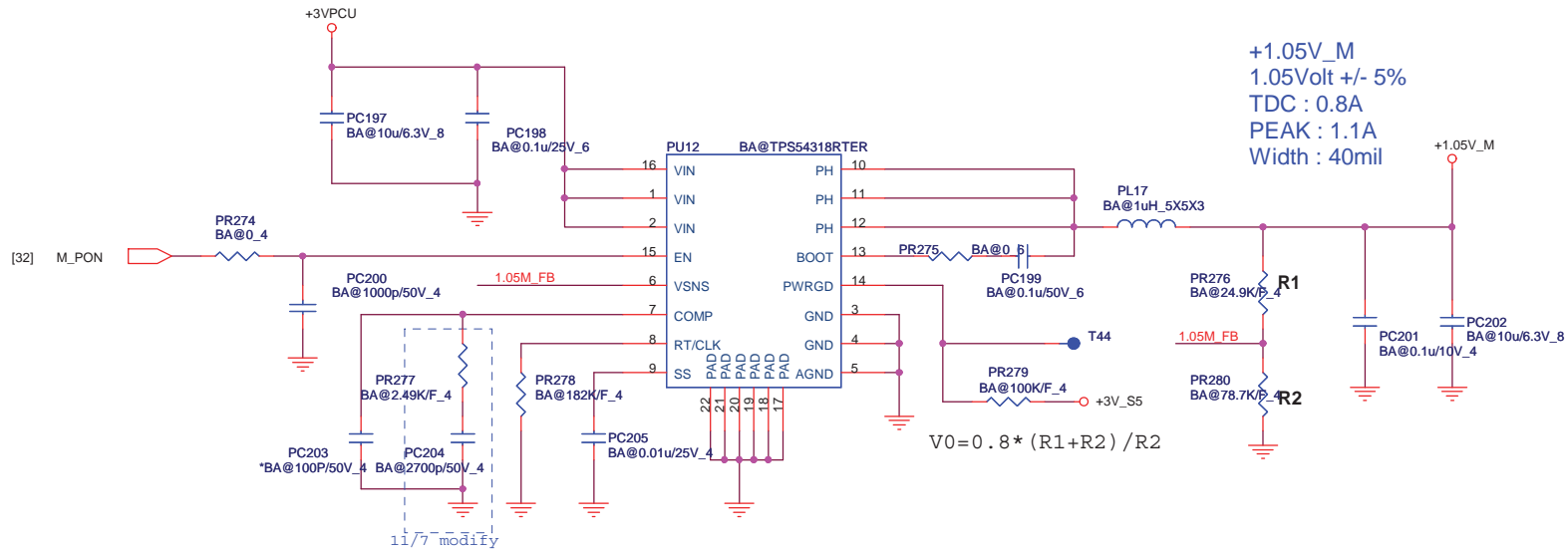




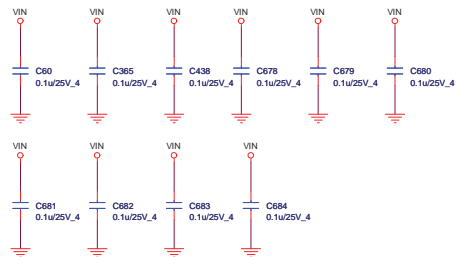
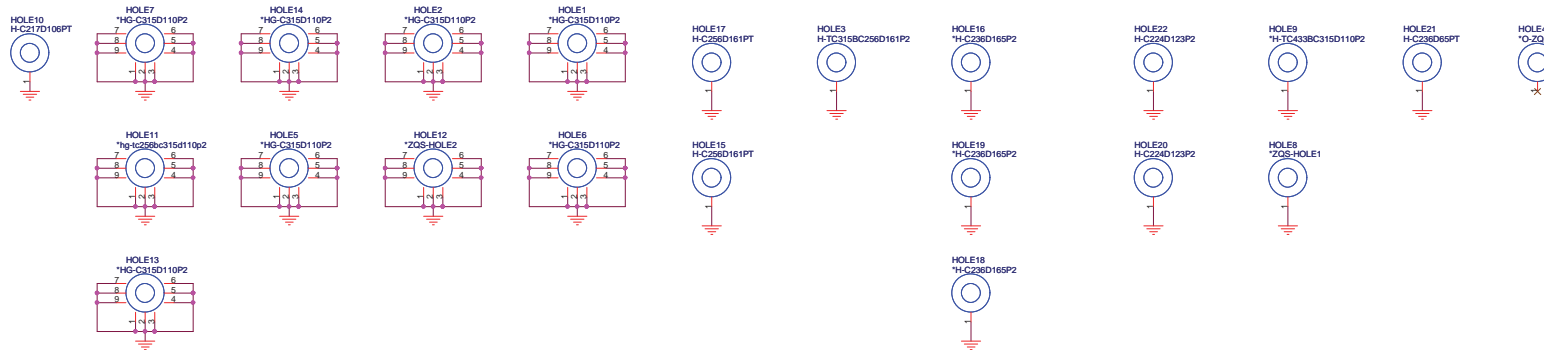
**Quanta Computer Inc.**  
PROJECT : ZQTA/ZQSA

Size	Document Number	Rev
	<b>GPU_PWR</b>	1A
Date:	Friday, November 11, 2011	Sheet 40 of 44





# Hole



Model	date	CHANGE LIST
ZASA/ZSQTA	9/26	page3 : add R511,R525,R527,R528,R529 for Discrete Only &PCH_JTAG_TDO net change pull-up from +3V_S5 to +1.05 rail
	9/27	Update power circuit Page19 : add C3777,C3778
	9/30	Page18 : add Q3508 for U7 GPU_THERMAL_ALERT net Page31 : Del CN1
	10/3	Page18 : add dGPU_ACDC# net to U7 GPIO04 & add R347 Page22 : add R557,R554 to pull-down & R548,R547 stuff for Discrete only Page25 : add R3693,C116 for ODD zero power circuit
	10/4	Page31 : CN8 add board id3 & board id4 net for touch pad ID control
	10/5	Page31 : CN8.2,CN8.3 add CLK_SDATA & CLK_SCLK net for touch pad & add R278,R279 Page15 : U41 Power rail change to +3V_GFX Page24 : Del Q16 no't support wake up function Page18 : add Q3509 for dGPU_ACDC# net Page31 : add L35,R3694,R3695 for touch pad 5V & 3V option & add R297,R295 Fan PWR option
	10/6	Page17 : IFPAB_PLLVDD rail change from +1.8V_GFX to +3V_GFX Page27 : U6 change footprint Page39 : PWR engineer add PQ3006,PQ3005 Page40 : PWR engineer Del PR193,PQ51,PQ54
	10/7	Page16 :add C3779,C3780 Page29 :add C542,C530 for EMI solution & C544 change to 4.7u 0603 type Page35 :PWR engineer add PC3037,PC3038,PC3039 Page35 :PWR engineer add PC3035,PC3036
	10/11	Page8 :add R376,R381,R393,R407,R421,R434 for Dual SPI ROM Page9 :U13 power rail change to +3V Page10 :SV_DET_NC net add R250 to pull-down Page27 :add R133,R235 Page30 :C443 change to 3528 type & add C366,R340 Page31 :CN2.27 pin change to +VGACORE Page32 :add R330,R328 pull-up +3VPCU for GPUT_CLK,GPUT_DATA net
	10/14	Page20 :add C3781,C3782,R3569,R3570,R3571,R3576 Page21 :add C3783,C3784,R3577,R3578,R3579,R3581



**Quanta Computer Inc.**  
PROJECT : ZQTA/ZQSA

DOC NO.

PROJECT MODEL :

ZQTA/ZQSA

APPROVED BY:

DATE:

PART NUMBER:

DRAWING BY:

REVISION:

Change list

Date: Friday, November 11, 2011 Sheet 44 of 44

Rev  
1A

[www.vinafix.vn](http://www.vinafix.vn)